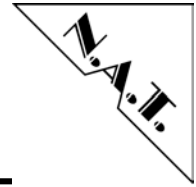


**NPMC-8260-4E1/T1
Telecom PMC Module
Technical Reference Manual V1.15
HW Revision 1.5**

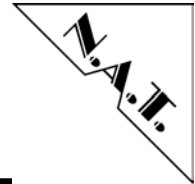


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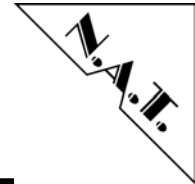
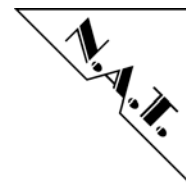
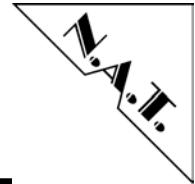


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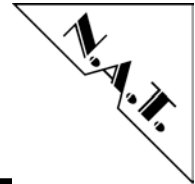


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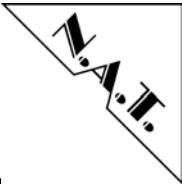
Conventions

If not otherwise specified, addresses and memory maps are written in hexadecimal notation, identified by *0x*.

Table 1 gives a list of the abbreviations used in this document:

Table 1: List of used abbreviations

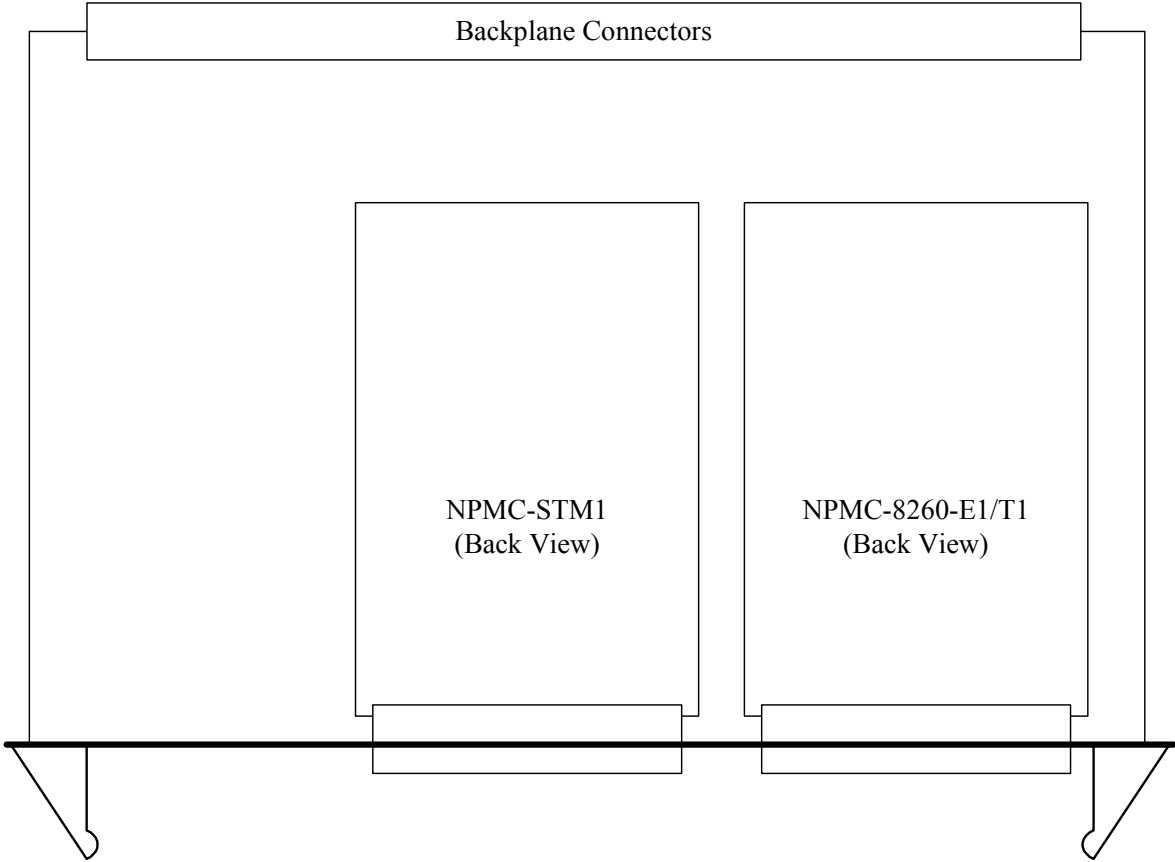
Abbreviation	Description
60x bus	PowerPC processor bus
b	Bit, binary
B	byte
CPU	Central Processing Unit
DMA	Direct Memory Access
E1	2.048 Mbit G.703 Interface
Flash	Programmable ROM
H.110	Time-Slot Interchange Bus
J1	1,544 Mbit G.703 Interface (Japan)
K	kilo (factor 400 in hex, factor 1024 in decimal)
LIU	Line Interface Unit
M	mega (factor 10,000 in hex, factor 1,048,576 in decimal)
MHz	1,000,000 Herz
MPC8260	Embedded processor from Motorola
PowerQUICC II	MPC8260, MPC8255
PowerSpan (II)	Tundra PCI-Bus Controller
RAM	Random Access Memory
ROM	Read Only Memory
SCbus	Time-Slot Interchange Bus of the SCSA, subset of H.110 bus
SCC	Serial Communication Controller of the MPC8260
SCSA	Signal Computing System Architecture
SDRAM	Synchronous Dynamic RAM
SMC	Serial Communication Controller of the MPC8260
SRAM	Static RAM
T1	1,544 Mbit G.703 Interface (USA)
TDM	Time Division Multiplex
TSI	Time Slot Interchange

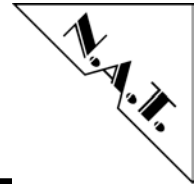


1 Introduction

The NPMC-8260-4E1/T1 is a high performance standard CPU PCI Mezzanine Card Type 1. It can be plugged onto any carrier board supporting PMC standards:

Figure 1: NPMC-8260-4E1/T1 on a carrier board (VMEbus, cPCI)

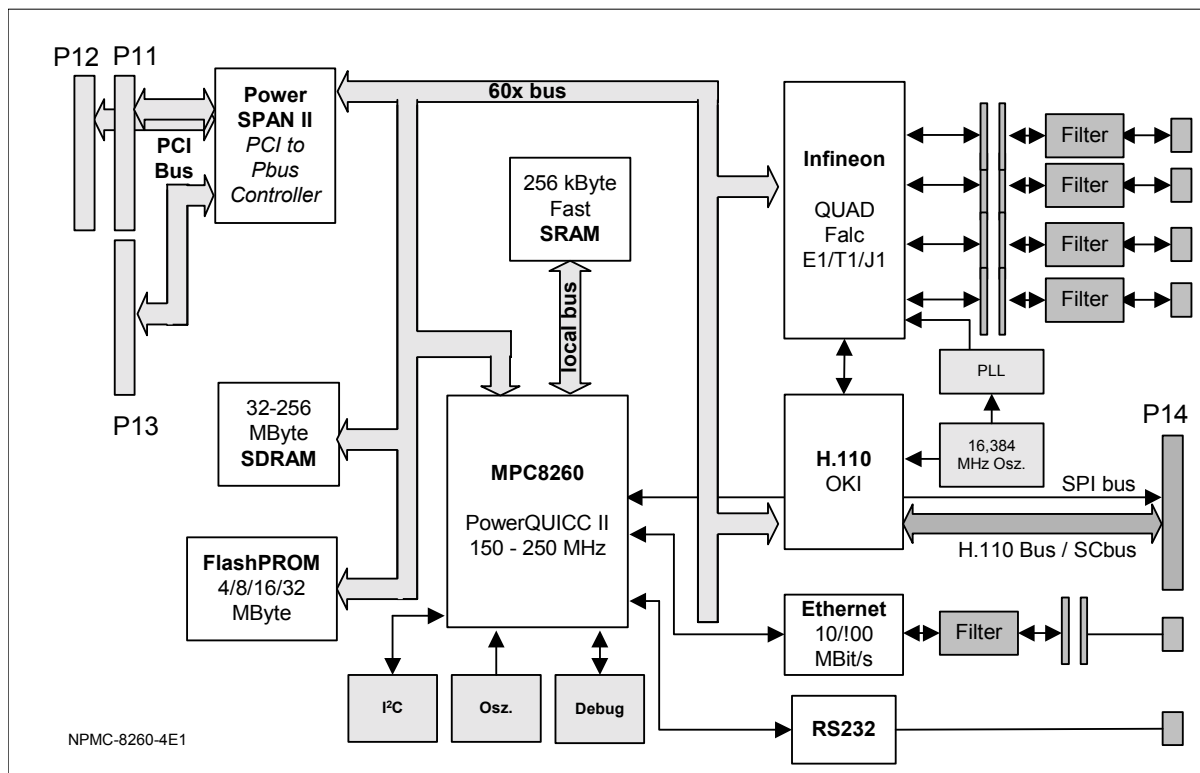


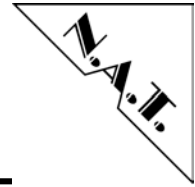


The NPMC-8260-4E1/T1 has the following major features on-board:

- PowerQUICC II MPC8260 based Embedded PowerPC Architecture
- Front-panel I/O
- 64 bit / 66 MHz PCI Bus interface Rev. 2.2
- 4 x E1 / T1 / J1 primary rate line interface
- 100BaseT Ethernet channel
- H.110 / SCSA TSI bus
- SPI bus
- 32 – 256 MB main memory (SDRAM)
- 512 KB fast SRAM on local bus
- 4 – 32 MB FLASH

Figure 2: NPMC-8260-4E1/T1 Block Diagram





1.1 Board Features

- **CPU**

Depending on the assembled CPU the PowerQUICC II runs with a core clock frequency of 150 - 300 MHz. The user may choose between a MPC8260 or a MPC8255 CPU (assembly option).

- **Memory**

SDRAM: The **NPMC-8260-4E1/T1** provides 32 to 256 MB SDRAM onboard. The SDRAM is installed as a SODIMM SDRAM module. PC100-type modules of 32 MB, 64 MB, 128 MB, and 256 MB are supported. The SDRAM is 64 bit wide.

Default: 32 MB installed

Flash PROM: The 16-bit wide Flash PROM provides a capacity of 4 - 32 MB (assembly option).

Default: 16 MB installed

SRAM: There is a fast, synchronous SRAM connected to the local bus of the MPC8260 CPU. This fast memory, which does not have to be arbitrated, can be used for descriptor tables, etc.. It is 32 bit wide and either 128 KB, 256 KB, or 512 KB in size (assembly option).

Default: 512 KB installed

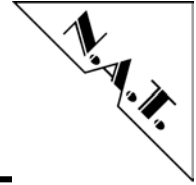
- **Interfaces**

PCI: The **NPMC-8260-4E1/T1** includes a 32/64 bit 33/66 MHz PCI bus interface. This is implemented by a Tundra CA91L8260B PowerSpan II device.

Note: Early access boards implement a CA91L8260 PowerSpan.

H.110: The **NPMC-8260-4E1/T1** implements a 32bit H.110 interface, which includes a SCbus interface on I/O-connector P14 according to PMC specifications. This is implemented by an OKI ML53812-2 TSI device.

Note: The SL0-4 SCbus address lines on the PMC I/O connector P14 are not 5V tolerant on early access boards (HW Rev. 1.2 and less). Please supply with 3.3V signaling if SL0-4 are to be used! Fixed in HW Rev. 1.3 and higher.



SPI: The **NPMC-8260-4E1/T1** implements a SPI bus interface on the PMC I/O connector P14

Note: The SPI bus lines on the PMC I/O connector P14 are not 5V tolerant on early access boards (HW Rev. 1.2 and less). Please supply with 3.3V signaling if SPI bus is to be used!
Fixed in HW Rev. 1.3.

- **I/O**

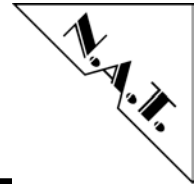
E1/T1/J1: The module carries a PEB22554 (QuadFALC) framer, which implements four E1/T1/J1 interfaces.

Ethernet: The 100 Mbit Ethernet MII interface supplied by the PowerQUICC II is connected to a 100BaseT interface through a LXT972 framer device.

RS232: There are 2 RS232 interfaces available on the **NPMC-8260-4E1/T1**:

- a RS232 interface (SCC1)
- a RS232 interface (SMC1) sharing a connector with the BDM / JTAG interface

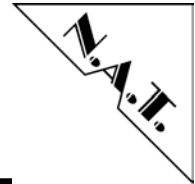
Note: The 4 E1/T1-, the RS232-, and the Ethernet line interfaces are connected to front panel connectors. The H.110/SCbus is connected to the PCI I/O connector.



1.2 Board Specification

Table 2: NPMC-8260-4E1/T1 Features

Processor	PowerQUICC II MPC8260 or MPC8255 based Embedded PowerPC Architecture, 150 to 250 MHz
PMC-Module	Standard PCI Mezzanine Card Type 1
PCI to QBUS bridge	PowerSPAN II
Front-I/O	3 RJ45 connectors
Main Memory	32 - 256 MByte SDRAM PC100-type
Flash PROM	4 – 32 MByte Flash PROM. On board programmable
Local Memory	128 / 256 / 512 Kbyte fast SRAM on local bus
Firmware	OK1, VxWorks BSP (on request)
Power consumption	3.3V 0.5A typ. 5.0V 0.8A typ.
Environmental conditions	Temperature (operating): 0°C to +60°C with forced cooling Temperature (storage): -40°C to +85°C Humidity: 10 % to 90 % rh noncondensing
Standards compliance	PCI Rev. 2.2 P1386.1 / Draft 2.4a



2 Installation

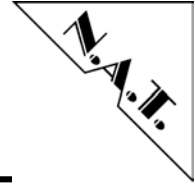
2.1 Safety Note

To ensure proper functioning of the **NPMC-8260-4E1/T1** during its usual lifetime take the following precautions before handling the board.

CAUTION

Electrostatic discharge and incorrect board installation and uninstallation can damage circuits or shorten their lifetime.

- Before installing or uninstalling the **NPMC-8260-4E1/T1** read this installation section
- Before installing or uninstalling the **NPMC-8260-4E1/T1**, read the Installation Guide and the User's Manual of the carrier board used
- Before installing or uninstalling the **NPMC-8260-4E1/T1** on a carrier board or both in a rack:
 - Check all installed boards and modules for steps that you have to take before turning on or off the power.
 - Take those steps.
 - Finally turn on or off the power.
- Before touching integrated circuits ensure to take all require precautions for handling electrostatic devices.
- Ensure that the **NPMC-8260-4E1/T1** is connected to the carrier board via all PMC connectors and that the power is available on both PMC connectors (GND, +5V, and +3,3V).
- When operating the board in areas of strong electromagnetic radiation ensure that the module
 - is bolted the front panel or rack
 - and shielded by closed housing



2.2 Installation Prerequisites and Requirements

IMPORTANT

Before powering up

- check this section for installation prerequisites and requirements

2.2.1 Requirements

The installation requires only

- a carrier board for connecting the **NPMC-8260-4E1/T1**
- power supply

2.2.2 Power supply

The power supply for the **NPMC-8260-4E1/T1** must meet the following specifications:

- required for the module:
 - +3,3V / 1,0A typical
 - +5,0V / 1,0A typical

2.2.3 Automatic Power Up

In the following situations the **NPMC-8260-4E1/T1** will automatically be reset and proceed with a normal power up.

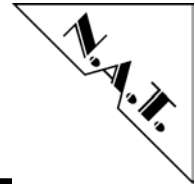
Voltage sensors

The voltage sensor generates a reset

- when +5V voltage level drops below 4,4V *
- when +5V voltage level rises above 5,6V *
- when +3.3V voltage level drops below 2,65V *
- when +3.3V voltage level rises above 3,9V *
- or when the carrier board signals a PCI Reset

Watchdog (if enabled)

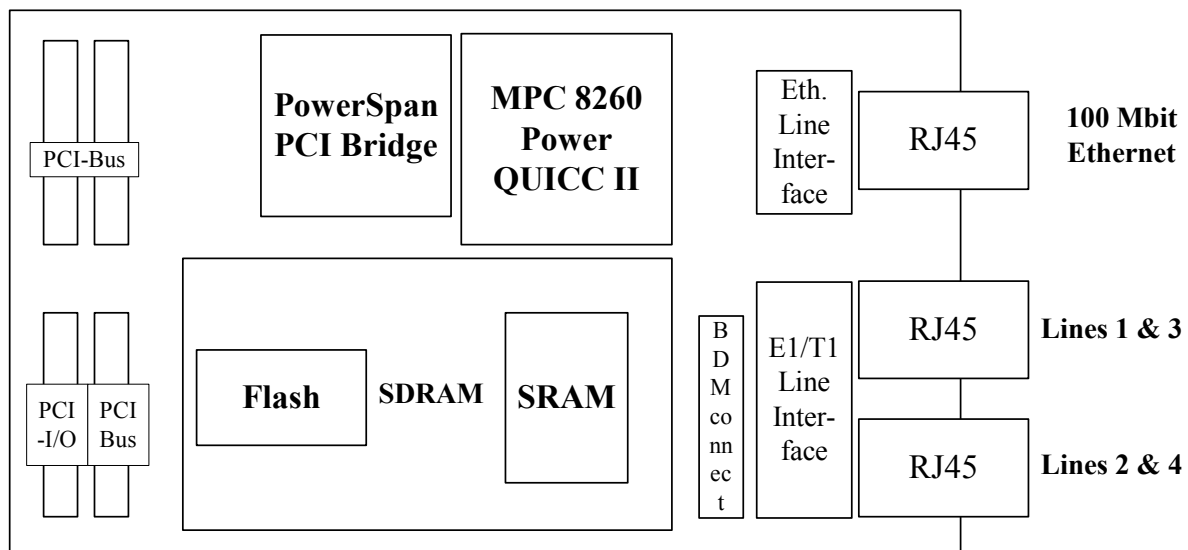
* defined by: “PCI Specification Revision 2.2, Section 4.2.1.1 and Section 4.3.2”



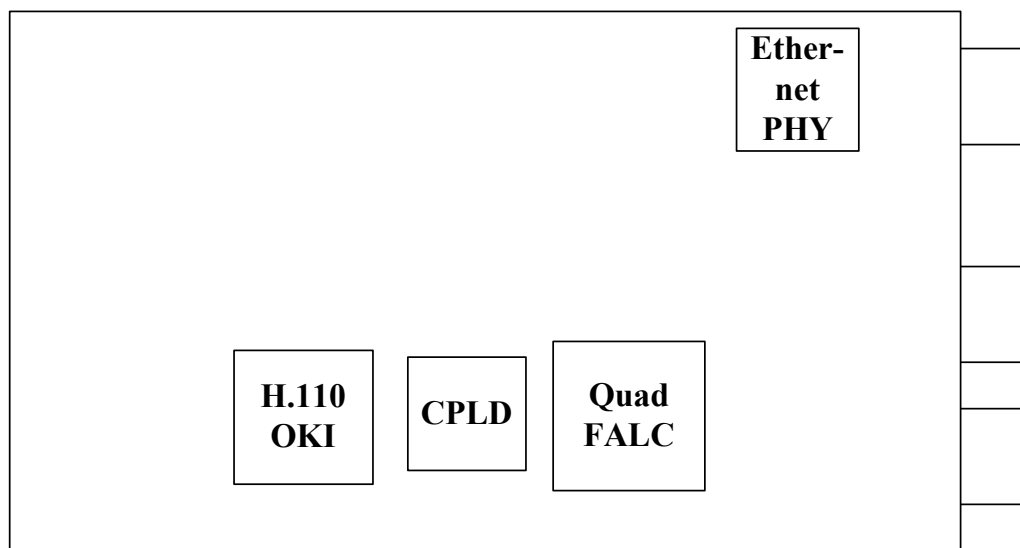
2.3 Location Overview

The figure 3 "Location diagram of the NPMC-8260-4E1/T1" highlights the position of the important components. Depending on the board type it might be that the board does not include all components named in the location diagram.

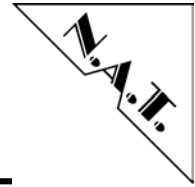
Figure 3: Location diagram of the NPMC-8260-4E1/T1



Top View



Bottom View



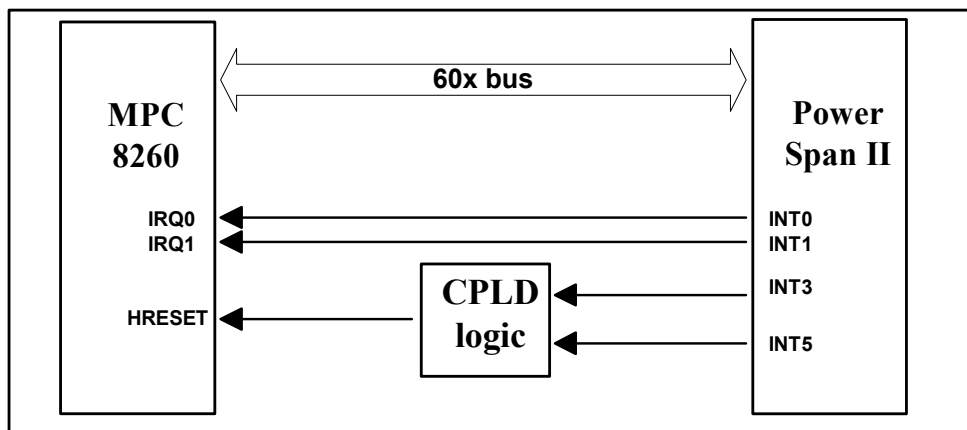
3 Functional Blocks

The NPMC-8260-4E1/T1 can be divided into a number of functional blocks, which are described in the following paragraphs.

3.1 PCI Interface

The NPMC-8260-4E1/T1 includes a 32/64 bit 33/66 MHz PCI bus interface. This is implemented by a Tundra CA91L8260B PowerSpan II device. The PowerSpan connects to the 64-bit-wide 60x bus of the MPC8260 processor. It passes PCI Reset from the host to the PMC module, handles interrupts both ways to and from the module, and allows access from the host to resources onboard the module as well as from the module to host memory. Appropriate register setup and memory window definitions have to be performed by the host CPU.

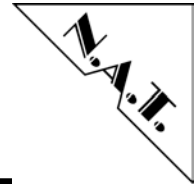
Figure 4: Interface PowerSpan / MPC8260



3.2 Processor

The MPC8260 PowerQUICC II™ is a versatile communications processor that integrates on one chip a high-performance PowerPC™ RISC microprocessor, a very flexible system integration unit, and many communications peripheral controllers that can be used in a variety of applications, particularly in communications and networking systems.

The core is an embedded variant of the PowerPC MPC603e™ microprocessor with 16 Kbytes of instruction cache and 16 Kbytes of data cache and no floating-point unit (FPU). The system interface unit (SIU) consists of a flexible memory controller that interfaces to almost any user-defined memory system, and many other peripherals making this device a complete system on a chip.



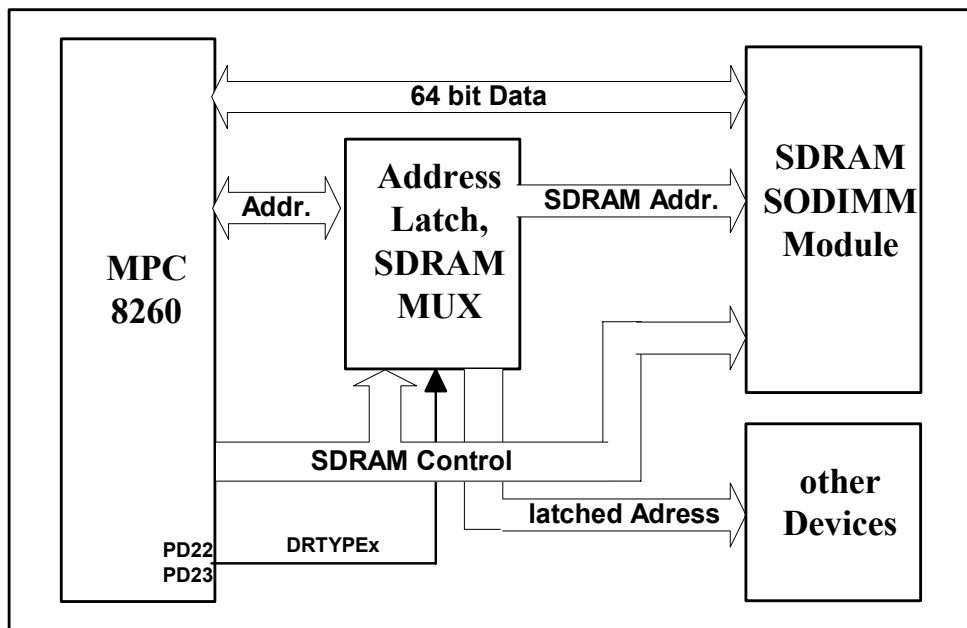
The communications processor module (CPM) includes four serial communications controllers (SCCs) , with the addition of three high-performance communication channels that support new emerging protocols (for example, 155-Mbps ATM and Fast Ethernet). The MPC8260 has dedicated hardware that can handle up to 256 full-duplex, time-division-multiplexed logical channels, as well as DMA functionality executing memory to memory and memory to I/O transfers.

3.3 Memory

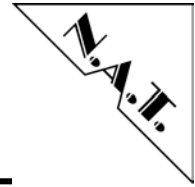
3.3.1 SDRAM

As the onboard SDRAM memory has to be accessed not only by the CPU, but also by the host through the PowerSpan PCI bridge, external address latches and multiplexers had to be implemented. The structure is shown in Figure 4 below.

Figure 5: Address / Data Paths to onboard Devices



The SDRAM is connected to the 60x bus interface of the MPC8260. The multiplexer organization can be adjusted to different SDRAM types by the DRTYPEx selection signals. Suitable SDRAM modules must be of PC100 or PC133 type. Refer to **Chapter 4, Table 10:** and **Table 11:** for further information on SODIMM modules.



3.3.2 FLASH

FLASH memory is connected to the upper 16 data bits D0 – 15 and to the latched address lines. The FLASH on the NPMC-8260-E1/T1 can be programmed either by the CPU (by appropriate software or through the BDM port) or by a PCI bus master through the PowerSpan PCI bridge. In the latter case the PowerQUICC II has to be prevented from booting from FLASH while this does not contain a defined boot program, in order not to enter unknown states. This can be achieved by installing a jumper (JP3), which disables the MPC8260 CPU core after the following Power-Up cycle. This feature is used for programming the FLASH memory via the PCI bus. If JP3 is installed the Hardware Configuration Words for the CPU and the PowerSpan are loaded from an onboard CPLD. If JP3 is not installed, the Hardware Configuration Words are loaded from the first 128 bytes of the FLASH. Once the FLASH has been programmed, it may be reprogrammed without having to install JP3. Programming software is available on request. Please refer to section 5.4 for details on jumper JP3.

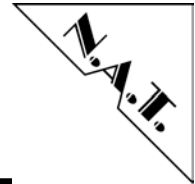
3.3.3 SRAM

The 32-bit wide, synchronous SRAM is connected to the local bus interface of the PMC8260.

3.3.4 I²C Devices

There are two I²C devices on the **NPMC-8260-4E1/T1**, which are connected to the MPC8260 I²C bus; an EEPROM used for storage of board-specific information, and the EEPROM on the SODIMM SDRAM module, which contains vital data about the SDRAM module size and address organisation. This information is necessary, in order to be able to program the SDRAM controller functions appropriately. The EEPROM on the SODIMM typically defaults to a 24C02 type, the EEPROM for storage of board-specific information defaults to a 24C08 device. The address of the EEPROM on the SDRAM SODIMM module is 0x0, the address of the other EEPROM is 0x4.

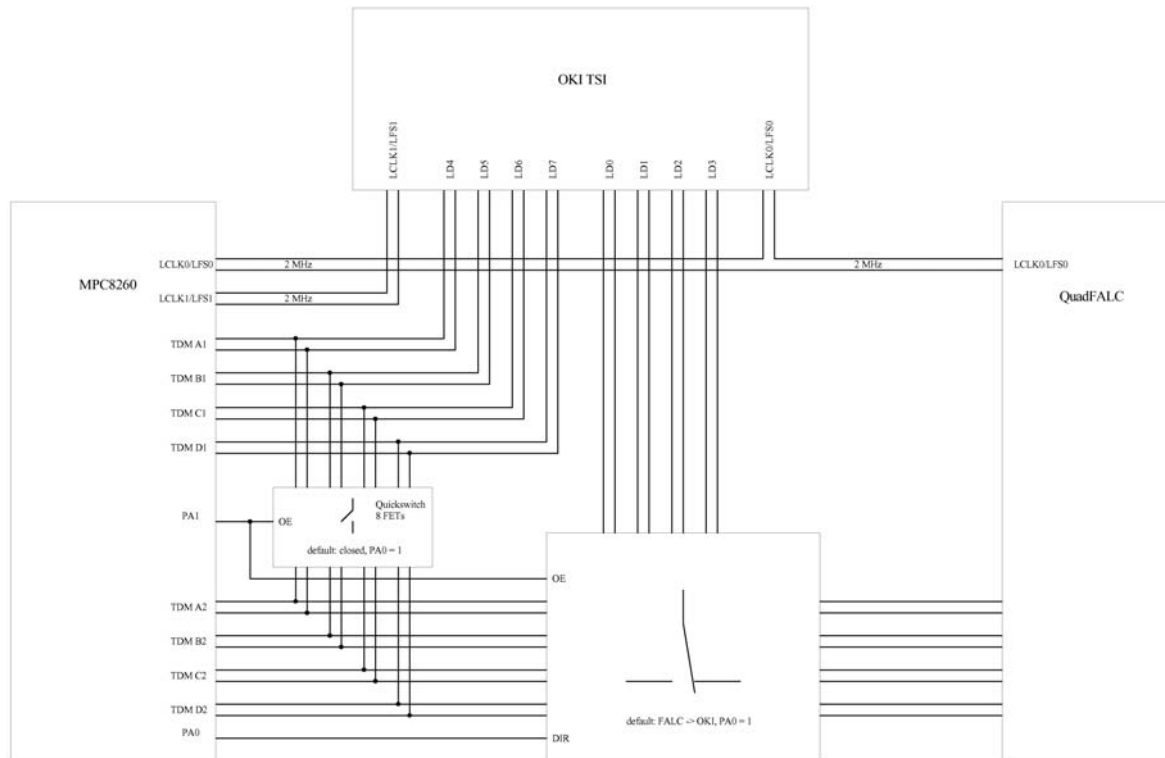
Another I²C device (24C02) connects to the PowerSpan. The PowerSpan reads its basic register setup information from this EEPROM on Reset. The memory area above 0x40 is not used by the PowerSpan and may be used for additional user configuration data.



3.4 H.110 Bus Controller and Line Interfaces

3.4.1 Block Diagramm of the TDM Structure

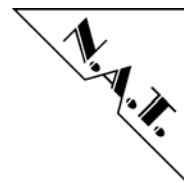
Figure 6: Local TDM Bus Organisation and Synchronisation



3.4.2 Description of the TDM Structure

The TDM data are routed through the ML53812-2 TSI device. Hence, any timeslot switching between H.110 bus, framers, and CPU is possible. Local TDM data lines LDI[0 – 3] and LDO[0 – 3] are routed between QuadFALC and TSI and CPU. In order to prevent data distortion the data outputs of the QuadFALC may be isolated from the TDM bus, if all 8 TDM lines are to be used between TSI and CPU. The switch element connecting the QuadFALC data lines LDI[0 – 3] is enabled by programming CPU port pin PA0. Default: PA0 = 1, QuadFALC data lines LDI[0 – 3] enabled.

For compatibility reasons to earlier versions of the **NPMC-8260-4E1/T1** there is another switch element that connects MPC8260's TDMx1 signals with TDMx2 signals. This feature is enabled by programming CPU port pin PA1. Default: PA1 = 1, MPC8260's TDMx1 signals connected to with TDMx2 signals.



The connection between the TDM data lines LDI[0 – 7] / LDO[0 – 7] and the corresponding TDM channels of the MPC8260 for PA1 = 0 is shown in the following table:

Table 3: TDM Channel ↔ LDI/O Data Line Connection

MPC8260 TDM Channel	TDM data line LDIx/LDOx	Sync for TDM Channel	Clock for TDM Channel
TDM_A1	LDI/O[4]	L_FS0	L_CLK0
TDM_B1	LDI/O[5]	L_FS0	L_CLK0
TDM_C1	LDI/O[6]	L_FS0	L_CLK0
TDM_D1	LDI/O[7]	L_FS0	L_CLK0
TDM_A2	LDI/O[0]	L_FS1	L_CLK1
TDM_B2	LDI/O[1]	L_FS1	L_CLK1
TDM_C2	LDI/O[2]	L_FS1	L_CLK1
TDM_D2	LDI/O[3]	L_FS1	L_CLK1

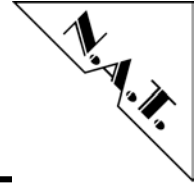
The connection between the TDM data lines LDI[0 – 7] / LDO[0 – 7] and the corresponding TDM channels of the MPC8260 for PA1 = 1 is shown in the following table:

Table 4: TDM Channel ↔ LDI/O Data Line Connection

MPC8260 TDM Channel	TDM data line LDIx/LDOx	Sync for TDM Channel	Clock for TDM Channel
TDM_A1	LDI/O[4]	L_FS0	L_CLK0
TDM_B1	LDI/O[5]	L_FS0	L_CLK0
TDM_C1	LDI/O[6]	L_FS0	L_CLK0
TDM_D1	LDI/O[7]	L_FS0	L_CLK0
TDM_A2	LDI/O[4]	L_FS1	L_CLK1
TDM_B2	LDI/O[5]	L_FS1	L_CLK1
TDM_C2	LDI/O[6]	L_FS1	L_CLK1
TDM_D2	LDI/O[7]	L_FS1	L_CLK1

The Sync and Clock signals L_FS[0-1] and L_CLK[0-1] can be programmed within the OKI TSI local clock and local sync settings.

The TSI device derives its time base from one of the LREF signals coming from the framers, or from the H.110 bus. From this input it generates local clock and frame sync for the framers and the CPU to synchronize to. Timing reference for offboard routing devices can be provided by programming one of the local LREF signals to be output on one of the NETREFx signals. For detailed information please refer to the Motorola MPC8260, OKI ML53812-2, and Infineon PEB22554 User’s Manuals.



3.4.3 SCbus Compatibility

The SCbus implemented on the NPMC-8260-E1/T1 is a sub-set of the H.110 bus. SCbus data lines correspond to H.110 data lines CT_D[0 – 15]. See chapter 5.8 (PMC P14 Connector) for reference. As an assembly option either the H.110 reference signal NETREF1 or NETREF2 may be connected to the corresponding SCbus signal SREF_8K.

By default, NETREF1 is connected to SREF_8K.

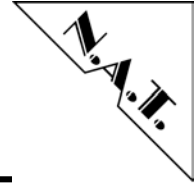
3.4.4 E1/T1/J1 Line Interfaces

The four E1/T1/J1 interfaces connect the Infineon QuadFLC framer to the front panel RJ45 connectors. Timing and interface characteristics can be set up by software within the QuadFALC, the correct line impedance is selected by programming the IMPSELA and IMPSELB port signals as described below in chapter 4. The line interfaces conform to EN60950 and G.703.

3.5 Ethernet

The LXT972 Ethernet LIU is connected to the MPC8260 through the MII interface. It shares the front panel connector S3 with the RS232 debug interface, depending on an assembly option. By default, Ethernet is enabled and RS232 is disabled on connector S3.

Configuration settings of the LXT972 are done by MPC8260 port pins. This applies to signals TxSLEW_x, PAUSE, and PWRDWN. Refer to Table 9: for details. ADDR0 is grounded.



4 Hardware

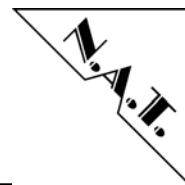
4.1 Memory Map

All addresses are set up by programming the corresponding Chip-Select Decoder of the PowerQUICC.

Table 5: Memory Map

Device	CS Line	Address	Function	Notes
Flash-PROM	CS0	programmable	Boot, user code	4/8/16/32 MByte Flash-Prom (16 bit wide)
not used	CS1			
SDRAM	CS2	programmable	main memory, CS2 and CS3 share the same SODIMM	32 - 256 MByte SDRAM (64 bit wide)
SDRAM	CS3	programmable		
not used	CS4			
ML53812 TSI	CS5	programmable	H.110	8 bit wide
PEB22554	CS6	programmable	QuadFALC	8 bit wide
Registers	CS7	programmable	internal registers	8 bit wide
SRAM	CS8	programmable	SRAM (on local bus)	128 / 256 / 512 kByte SRAM (32 bit wide)
SRAM	CS9	programmable		
not used	CS10			
not used	CS11			
CA91L8260B	none*	programmable	PowerSpan II	64 bit wide

* The PowerSpan's base address on PBus is loaded from the serial I²C EEPROM accompanying the PowerSpan. The EEPROM long load sequence used on the NPMC-8260-4E1/T1 initializes the register base address on PBus to be 0x1000.0000. No CS logic is used to access the PowerSpan.

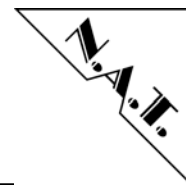


4.2 Definition of PowerQUICC II Port Pins

PowerQUICC II port pins are used to communicate with the framers and to set up some board configuration. In detail:

Table 6: PowerQUICC II Port Pin Usage (Port A)

Signal Function	PowerQUICC II Port A Pin	Description
Ethernet MII COL	PA31	MII interface to the 100 Mbit transceiver LXT972
Ethernet MII CRS	PA30	MII interface
Ethernet MII TX ER	PA29	MII interface
Ethernet MII TX EN	PA28	MII interface
Ethernet MII RX DV	PA27	MII interface
Ethernet MII RX ER	PA26	MII interface
Ethernet MII MDC	PA25	MII interface
Ethernet MII MDIO	PA24	MII interface
	PA23	
	PA22	
Ethernet MII TXD3	PA21	MII interface
Ethernet MII TXD2	PA20	MII interface
Ethernet MII TXD1	PA19	MII interface
Ethernet MII TXD0	PA18	MII interface
Ethernet MII RXD3	PA17	MII interface
Ethernet MII RXD2	PA16	MII interface
Ethernet MII RXD1	PA15	MII interface
Ethernet MII RXD0	PA14	MII interface
	PA13	
	PA12	
	PA11	
	PA10	
TSI LDI4	PA9	Time Slot Assigner Bus data bit 4, output of the MPC8260, input to the ML53812 H.110 controller (Time Slot Interchange (TSI))
TSI LDO4	PA8	Time Slot Assigner Bus data bit 4, input to the MPC8260, output of the ML53812 H.110 controller (Time Slot Interchange (TSI))
TSI L_FS0	PA7	Time Slot Assigner frame sync, input to the MPC8260, output of the ML53812 H.110 controller
TSI L_FS0	PA6	TSA frame sync
	PA5	
	PA4	



TSI L_CLK1	PA3	Time Slot Assigner alternate clock, input to the MPC8260, output of the ML53812 H.110 controller
TSI L_CLK1	PA2	TSA alternate clock
TDM_DP1*	PA1	setup TDM data path between the TSI data lines, the MCCs, the QuadFALC
TDM_DP0*	PA0	setup TDM data path between the TSI data lines, the MCCs, the QuadFALC

Table 7: PowerQUICC II Port Pin Usage (Port B)

Signal Function	PowerQUICC II Port B Pin	Description
TSI LDI1	PB31	TSA data bus bit 1, TSI in
TSI LDO1	PB30	TSA data bus bit 1, TSI out
TSI L_FS1	PB29	TSA alternate frame sync
TSI L_FS1	PB28	TSA alternate frame sync
TSI LDI2	PB27	TSA data bus bit 2, TSI in
TSI LDO2	PB26	TSA data bus bit 2, TSI out
TSI L_FS1	PB25	TSA alternate frame sync
TSI L_FS1	PB24	TSA alternate frame sync
TSI LDI3	PB23	TSA data bus bit 3, TSI in
TSI LDO3	PB22	TSA data bus bit 3, TSI out
TSI L_FS1	PB21	TSA alternate frame sync
TSI L_FS1	PB20	TSA alternate frame sync
	PB19	
	PB18	
TSI L_CLK1	PB17	TSA alternate clock
TSI L_CLK1	PB16	TSA alternate clock
TSI LDI6	PB15	TSA data bus bit 6, TSI in
TSI LDO6	PB14	TSA data bus bit 6, TSI out
TSI L_FS0	PB13	TSA frame sync
TSI L_FS0	PB12	TSA frame sync
TSI LDI7	PB11	TSA data bus bit 7, TSI in
TSI LDO7	PB10	TSA data bus bit 7, TSI out
TSI L_FS0	PB9	TSA frame sync
TSI L_FS0	PB8	TSA frame sync
TSI LDI0	PB7	TSA data bus bit 0, TSI in
TSI LDO0	PB6	TSA data bus bit 0, TSI out
TSI L_FS1	PB5	TSA alternate frame sync
TSI L_FS1	PB4	TSA alternate frame sync

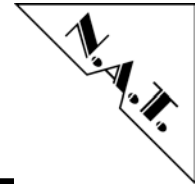


Table 8: PowerQUICC II Port Pin Usage (Port C)

Signal Function	PowerQUICC II Port C Pin	Description
TSI L_CLK0	PC31	Time Slot Assigner clock, input to the MPC8260, output of the ML53812 H.110 controller
TSI L_CLK0	PC30	TSA clock
TSI L_CLK0	PC29	TSA clock
TSI L_CLK0	PC28	TSA clock
TSI L_CLK0	PC27	TSA clock
TSI L_CLK0	PC26	TSA clock
TSI L_CLK0	PC25	TSA clock
TSI L_CLK0	PC24	TSA clock
	PC23	
Ethernet MII TXCLK	PC22	MII interface
	PC21	
Ethernet MII RXCLK	PC20	MII interface
TSI L_CLK1	PC19	Time Slot Assigner alternate clock, input to the MPC8260, output of the ML53812 H.110 controller
TSI L_CLK1	PC18	TSA alternate clock
TSI L_CLK1	PC17	TSA alternate clock
TSI L_CLK1	PC16	TSA alternate clock
	PC15	
SL_4	PC14	SCbus slot address bit
SL_3	PC13	SCbus slot address bit
SL_2	PC12	SCbus slot address bit
SL_1	PC11	SCbus slot address bit
SL_0	PC10	SCbus slot address bit
IMPSELA*	PC9	E1/T1/J1 Interface and E1 Impedance Select
IMPSELB*	PC8	E1/T1/J1 Interface and E1 Impedance Select
	PC7	
	PC6	
LED6*	PC5	Front Panel LED 6
LED5*	PC4	Front Panel LED 5
LED4*	PC3	Front Panel LED 4
LED3*	PC2	Front Panel LED 3
LED2*	PC1	Front Panel LED 2
LED1*	PC0	Front Panel LED 1

Signals with asterisk (*) are described in detail below.

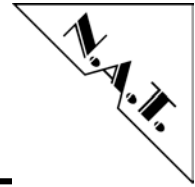
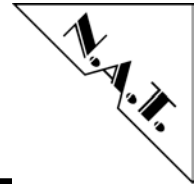


Table 9: PowerQUICC II Port Pin Usage (Port D)

Signal Function	PowerQUICC II Port D Pin	Description
RXD1_SCC*	PD31	receive data lines of the RS232 interface, SCC1
TXD1_SCC*	PD30	transmit data lines of the RS232 interface, SCC1
PAUSE*	PD29	LXT972 control function
	PD28	
TxSL1*	PD27	LXT972 control function
TxSL0*	PD26	LXT972 control function
	PD25	
PWRDN*	PD24	LXT972 control function
DRTYPE0*	PD23	SDRAM control function
DRTYPE1*	PD22	SDRAM control function
	PD21	
	PD20	
SPISEL	PD19	SPI Bus, Select
SPICLK	PD18	SPI Bus, Clock
SPIMOSI	PD17	SPI Bus, Data Out
SPIMISO	PD16	SPI Bus, Data In
SDA_PQ*	PD15	I ² C Bus, data
SCL_PQ*	PD14	I ² C Bus, clock
TSI LDI5	PD13	TSA data bus bit 7, TSI in
TSI LDO5	PD12	TSA data bus bit 7, TSI out
TSI L_FS0	PD11	TSA frame sync
TSI L_FS0	PD10	TSA frame sync
TXD1_SMC*	PD9	transmit data lines of the RS232 interface, SMC1
RXD1_SMC*	PD8	receive data lines of the RS232 interface, SMC1
	PD7	
	PD6	
	PD5	
E1/T1*	PD4	Framer Clock Select Signal



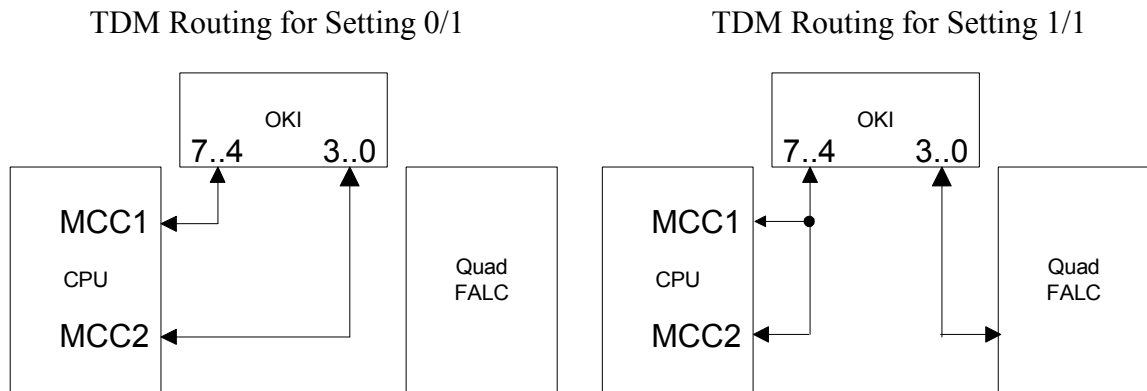
4.2.1 Signal Description

Port pins without signal name and description are not connected and should be programmed as outputs, signal level high, open drain.

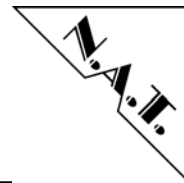
4.2.1.1 Selecting the TDM Data Path for MCC1 and MCC2

TDM_DP1, TDM_DP0 define the data paths between the TSI TDM data lines 0 – 3, the MCCs, and the QuadFALC. Refer to Figure 6: and to the drawings below for clarification. The following truth table applies:

TDM_DP1	TDM_DP0	TDM data routing
0	0	reserved for future use
0	1	MCC1 connects to OKI TDM data lines 4 – 7, MCC2 connects to OKI TDM data lines 0 – 3, QuadFALC disconnected
1	0	reserved for future use
1	1	MCC1 and MCC2 are shorted, connect to OKI TDM data lines 4 – 7, OKI TDM data lines 0 – 3 connect to QuadFALC (<i>default, V1.3 Mode</i>)



Note: This feature is available only from HW release 1.5 up. Earlier versions have TDM data lines 0 – 3 hard-wired between QuadFALC and CPU, and TDM data lines 4 – 7 hard-wired between CPU and OKI TSI.



4.2.1.2 Selecting the ISDN Line Impedance

IMPSELA, Line impedance select lines used for selection of 100 Ω (T1/J1),
 IMPSELB 120 Ω (E1), or 75 Ω (E1) receiver line termination

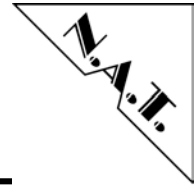
IMPSELA	IMPSELB	receiver line termination
0	0	100 Ω (T1/J1)
0	1	75 Ω (E1)
1	0	120 Ω (E1)
1	1	no termination selected <i>(default)</i>

4.2.1.3 I²C Interface Pins

SDA_PQ, I²C interface connected to the SDRAM SODIMM EEPROM (address 0x0)
 SCL_PQ and to the general purpose EEPROM U10 (24C02, address 0x4)

4.2.1.4 Serial Line Interface Pins

RXD1_SCC, receive data line of the RS232 interface, SCC1 on PD31
 TXD1_SCC transmit data line of the RS232 interface, SCC1 on PD30
 RXD1_SMC, receive data line of the RS232 interface, SMC1 on PD8
 TXD1_SMC transmit data line of the RS232 interface, SMC1 on PD9



4.2.1.5 100BaseT Configuration

TxSL0, TxSL1, Port pins used for LXT972 control functions. Please refer to the LXT972 users manual for details. Possible settings are:

TxSLEW1	TxSLEW0	slew rate (rise and fall time)
0	0	2.5 ns
0	1	3.1 ns
1	0	3.7 ns
1	1	4.3 ns (<i>default</i>)

PAUSE Port pin used for LXT972 control functions. Please refer to the LXT972 users manual for details.
Pause = 1: Pause capabilities during negotiation enabled (*default*)

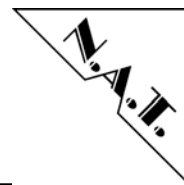
PWRDN Port pin used for LXT972 control functions. Please refer to the LXT972 users manual for details.
PWRDWN = 1: Power Down mode selected (*default*)

4.2.1.6 QuadFALC Clock Configuration Pin

E1/T1 clock select signal, defines the clock driven to the QuadFALC framer chip. The state of E1/T1 sets the input frequency of the analogue framer circuitry to be 1.544 MHz (E1/T1 = 0) or 2.048 MHz (E1/T1 = 1).

4.2.1.7 LED Control Pins

LED1 – LED6 Port pins used to control the front panel LEDs 1 – 6. Setting a port pin low (PCx = 0) turns the respective LED on, setting it high (PCx = 1) turns the respective LED off (*default*).



4.2.1.8 SDRAM Configuration Pins

DRTYPE0, Port pins used to set the correct multiplexing logic within Lattice U13.
DRTYPE1 These pins code the size and array information of the SDRAM module installed. The correct binary value for DRTYPE1-0 has to be determined by reading the SDRAM SODIMM EEPROM contents. This EEPROM contains also further information needed to program the SDRAM controller of the MPC8260 appropriately, e.g. row start address and clock cycles needed for SDRAM access.

DRTYPE_x settings refer to following SODIMM organisation:

Table 10: Supported SDRAM SODIMM Module Types

DRTYPE1 (PD22)	DRTYPE0 (PD23)	highest column address to be multiplexed	no. of SDRAM column addresses
0	0	SDA7	8
0	1	SDA8	9
1	0	SDA9	10
1	1	SDA11	11

SDA_x refers to SDRAM SODIMM address pin.

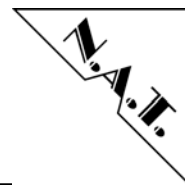
Addresses to be programmed as output for PowerQUICC II signals
 BNKSEL_x:

Table 11: BNKSEL_x Programming

DRTYPE1 (PD22)	DRTYPE0 (PD23)	BNKSEL2	BNKSEL1
0	0	PB_A19	PB_A20
0	1	PB_A18	PB_A19
1	0	PB_A17	PB_A18
1	1	PB_A16	PB_A17

PB_A_x refers to PowerQUICC II address line A_x. BNKSEL0 is not used.

Refer to chapter 7 of this manual and to the MPC8260 User’s Manual for a detailed description of how to program the Memory Controller of the MPC8260.



4.3 Interrupt Structure

The NPMC-8260-E1/T1 has the following Interrupt structure:

Table 12: Interrupt Structure

Interrupt source	PowerQUICC Interrupt level
PowerSpan II INT0	IRQ-Level 0 (highest level)
PowerSpan II INT1	IRQ-Level 1
ML53812	IRQ-Level 2
PEB22554	IRQ-Level 3
LXT972	IRQ-Level 4
NC	IRQ-Level 5
NC	IRQ-Level 6
NC	IRQ-Level 7 (lowest level)

The PowerSpan provides 6 interrupt pins, which may be programmed as incoming or outgoing interrupts (as seen from the PowerSpan). 4 of these are used as outgoing signals on the **NPMC-8260-4E1/T1**:

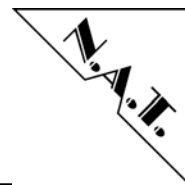
Table 13: PowerSpan Interrupt Pin Usage

PowerSpan Interrupt Pin	used as
INT0	PowerQUICC Interrupt level 0
INT1	PowerQUICC Interrupt level 1
INT2	not used
INT3	FLASH programming Mode
INT4	reserved
INT5	Software Reset to the PowerQUICC

Interrupt pins 3 and 5 are used as “Port Pins”, not as interrupts. If programmed as “doorbell interrupts”, they can be programmed to serve port-pin-like purposes.

Pin INT3 is used to invoke a special mode for FLASH programming, similar to the function of jumper JP3 described in chapter 6.3. Look there for further information.

Setting pin INT5 low generates a HRESET to the MPC8260 CPU. Please note that resetting the MPC8260 resets the PowerSpan as well, as both devices share the HRESET signal. Thus, after having reset the module by means of pin INT5, the PowerSpan needs to be initialised anew.



4.4 Register

Note: These registers are implemented from HW revisions 1.4 up. They are not available in earlier HW releases.

4.4.1 PCB Revision Register

There is an 8 bit wide PCB revision register implemented in the CPLD onboard the **NPMC-8260-4E1/T1**, which contains the revision code of the PCB. This code reads decimally-coded in 2 nibbles, i.e. the PCB version V1.0 reads 0x10. The register is addressed by the Register Chip Select CS7 as described in Table 5: with address offset 0x0.

4.4.2 I/O Register

There is an 8 bit wide I/O register implemented in the CPLD onboard the **NPMC-8260-4E1/T1**, which serves 3 functions:

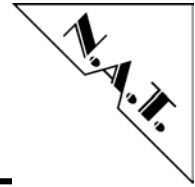
- software reset (reboot) functionality of the MPC8260 CPU, transformed by logic into a hardware reset to the CPU
- software reset of all I/O devices (QuadFALC, OKI TSI, Ethernet PHY)
- status of E1 or T1/J1 functionality for the QuadFALC, resulting in an appropriate MCLK (2.048 or 1.544 MHz) provided

The I/O register base address is programmed by the settings for CS4. The register is 8 bits wide, read/write, but only 2 bits are used, the rest reads as 0.

Table 14: I/O Register

Bit Number	Read/Write	Status Information / Control Setting
Bit 7	R/W	1 = reset for all I/O devices, defaults to 0
Bit 6	R	selection of E1 or T1/J1 functionality for the QFALC 0 = E1 (default), 1 = T1/J1
Bit 5	R	not used
Bit 4	R	not used
Bit 3	R	not used
Bit 2	R	not used
Bit 1	R	not used
Bit 0	W	1 = reset for the MPC8260 CPU, defaults to 0

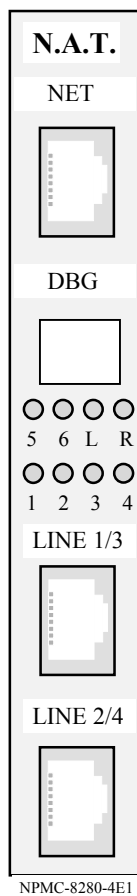
The register is addressed by the Register Chip Select CS7 as described in Table 5: with address offset 0x10.



4.5 Front Panel and LEDs

The NPMC-8260-4E1/T1 module is equipped with 12 LEDs, 10 of which are completely software programmable. Thus their functionality depends very much of the application running on the module.

Figure 7: Front Panel and LEDs



LEDs:

- LED R the red LED shows the processor Reset state:
LED lit indicates processor is in Reset state

- LED L this yellow LED shows the line status of the Ethernet connection:
LED lit shows link up.

- LED 6 - 1 the green LEDs 1 – 6 are fully software programmable and their meaning depends on user application.

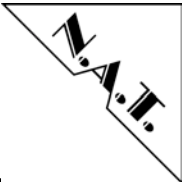
Connectors:

- NET The RJ45 connector S3 connects to an 100BaseT Ethernet network.

- DBG The Mini USB connector S4 connects to an RS232 debug interface.

- LINE 1/3, These RJ45 connectors S1 and S2 carry the 4 E1/T1/J1 interfaces. Each 2 interfaces share one connector.

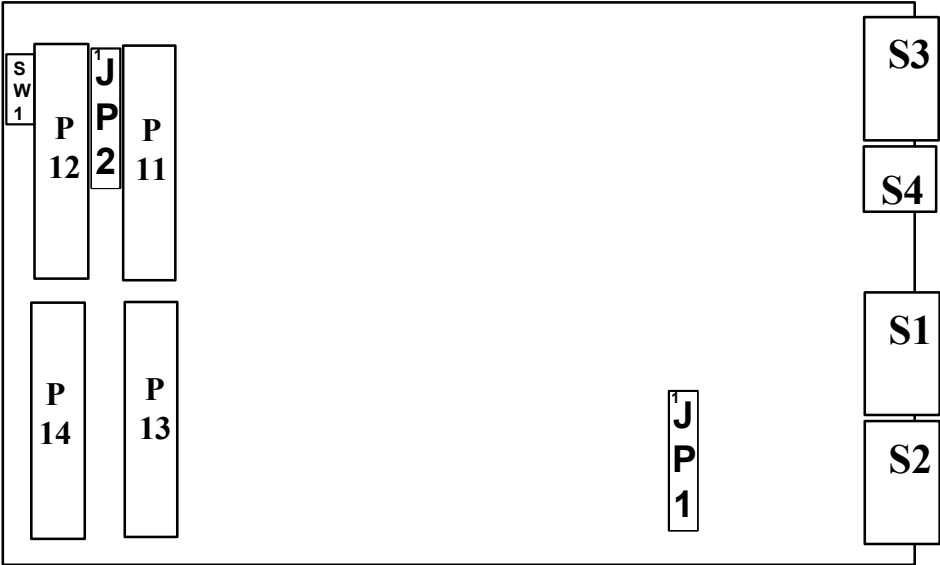
Please refer to Chapter 5.9 for details on front panel connectors.



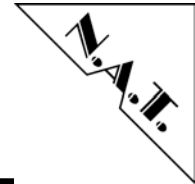
5 Connectors

5.1 Connector Overview

Figure 8: Connectors of the NPMC-8260-4E1/T1



Please refer to the following tables to look up the pin assignment of the NPMC-8260-4E1/T1.



5.2 Connector JP1: BDM and JTAG connector

The RS232 serial I/O port is available via a 20 pin SMD micro connector together with the JTAG / development Port / BDM Port (see JP1 in the location overview).

The RS232 port is realised with the PowerQUICC serial communication controller SMC1.

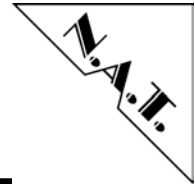
Table 15: Development Port / BDM and IEEE 1149.1 Connector Pinout

JTAG					
BDM Port					
PIN					
JP1					
TDO	TDO	1		2	/QACK
TDI	TDI	3		4	/TRST
	/QREQ	5		6	+3.3V
TCK	TCK	7		8	nc
TMS	TMS	9		10	nc
	/SRESET	11		12	GND
	/HRESET	13		14	nc
	/CHKSTOP OUT	15		16	GND
	RxD_SMC1	17		18	GND
	TxD_SMC1	19		20	GND

The BDM port (also called COP header) can be used for debugging. It is supported by major debug tool manufacturers.

Note: The BDM port is not assembled on normal production boards, as it is used only for debug purposes during kernel software development. If it is assembled, the connector JP1 slightly violates the height restrictions for PMC modules, which is 4.5mm at the location of JP1. If installed, JP1 is 5.5mm high.

An adapter board with cable plugging into the 20 pin SMD micro connector is available from N.A.T., that connects the JP1 connector to a standard 2-row, 16-pin, 100mil header used for BDM tool boxes, and routes the additional RS232 debug port signals to a standard 9-pin SubD female connector.

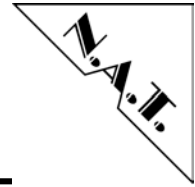


5.3 Connector JP2: Lattice programming port

Connector JP2 connects the JTAG- or programming-port of the Lattice CPLD devices. The CPLD devices are connected to a TDI – TDO daisy-chain.

Table 16: Lattice programming port

Pin No.	Signal	Signal	Pin No.
1	TCK	nc	2
3	TMS	GND	4
5	TDI	+3.3V	6
7	TDO	GND	8
9	/TRST	nc	10



5.4 Dual DIP Switch SW1

DIP Switch SW1 consists of 2 independent switches, which serve different functions. The numbers 1 and 2 of the switches is marked on the case.

5.4.1 Switch 1: EEPROM Write Protect Switch

If the PowerSPAN EEPROM shall be write-protected, this switch should be set to position “OFF”. This is the default factory setting. The EEPROM is preprogrammed and normally there is no need to alter the contents. If the EEPROM contents needs to be reprogrammed, set the switch to “ON”. After programming, set it to position “OFF” again, as there is a known bug with PowerSPAN II, which may corrupt the EEPROM if there is a power pailure while the EEPROM is read (like after Power-Up).

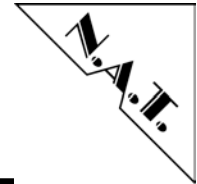
5.4.2 Switch 2: FLASH Programming Enable Switch

In order to program the FLASH via the PCI Bus, a special address translation has to take place, as the PowerSpan does not support dynamic bus sizing. There are two possible ways to enter this mode:

The first way to enter FLASH programming mode is chosen by setting switch 2 of SW1 to position “ON” and powering up the module. This mode is to be used in order to program a completely empty or corrupted FLASH device. The MPC8260 will read the configuration word from a CPLD device and come up in Core Disabled Mode, and the FLASH will be visible in the window programmed in the PowerSpan from PCI to 60x bus. After having programmed the FLASH, the switch has to be set to position “OFF” again and power needs to be cycled for the CPU to come out of Power-On-Reset with core enabled. This is the default factory setting.

The second way to enter FLASH programming mode is done by calling a software procedure that resets the MPC8260 and then brings it up in core disabled mode by programming two interrupt pins of the PowerSpan, which are used as I/O pins in this mode. This is the easier approach for software development, but will work only if the FLASH contains valid configuration word information already, as the MPC8260 needs to be operational for this mode to be invoked successfully. In this mode the MPC8260 can be restarted in core enabled mode by software.

As FLASH is only 16 bits wide, instead of the 64 bits of the 60x bus, and as there is no dynamic bus sizing, all data to be transferred has to be placed on the 2 highest bytes of the 64-bit wide word on the 60x bus. In order to achieve this, in programming mode all addresses accessed on the 60x bus are divided by 4 (shifted 2 bits to the right) by the CPLD logic, which latches the address to the FLASH and to I/O devices. The PowerSpan has to be set up appropriately by the programming software. Sample code is available on request.

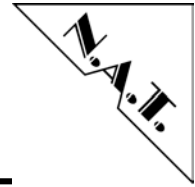


5.5 PMC Connector P11

Table 17: PMC Connector P11

Pin No.	PCI-Signal	PCI-Signal	Pin No.
1	TCK	-12V	2
3	GND	/INT A	4
5	/INT B	/INT C	6
7	/BUSMODE1	+5V	8
9	/INT D	PCI_RSV1	10
11	GND	3.3V _{aux}	12
13	CLK	GND	14
15	GND	/GNT	16
17	/REQ	+5V	18
19	V (I/O)	AD31	20
21	AD28	AD22	22
23	AD25	GND	24
25	GND	CBE3	26
27	AD22	AD21	28
29	AD19	+5V	30
31	V (I/O)	AD17	32
33	/FRAME	GND	34
35	GND	/IRDY	36
37	/DEVSEL	+5V	38
39	GND	/LOCK	40
41	/SDONE	/SB0	42
43	PAR	GND	44
45	V (I/O)	AD15	46
47	AD12	AD11	48
49	AD09	+5V	50
51	GND	/CBE0	52
53	AD06	AD05	54
55	AD04	GND	56
57	V (I/O)	AD03	58
59	AD02	AD01	60
61	AD00	+5V	62
63	GND	/REQ64	64

Pins for –12V, V_{aux}, and V(I/O) are not connected to the module. The same applies to JTAG signal TCK and PCI signals /LOCK, /SDONE, /SBO, /INTB, /INTC, /INTD. The PCI bridge chip always drives signals to 3.3V level, but it 5V tolerant.

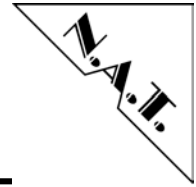


5.6 PMC Connector P12

Table 18: PMC Connector P12

Pin No.	PCI-Signal	PCI-Signal	Pin No.
1	+12V	/TRST	2
3	TMS	TDO	4
5	TDI	GND	6
7	GND	PCI_RSV3	8
9	PCI_RSV	PCI_RSV4	10
11	/BUSMODE2	+3.3V	12
13	/PCIRST	/BUSMODE3	14
15	+3.3V	/BUSMODE4	16
17	/PME	GND	18
19	AD30	AD29	20
21	GND	AD26	22
23	AD24	+3.3V	24
25	IDSEL	AD23	26
27	+3.3V	AD20	28
29	AD18	GND	30
31	AD16	/CBE2	32
33	GND	PCI_RESVD	34
35	/TRDY	+3.3V	36
37	GND	/STOP	38
39	/PERR	GND	40
41	+3.3V	/SERR	42
43	/CBE1	GND	44
45	AD14	AD13	46
47	M66EN	AD10	48
49	AD08	+3.3V	50
51	AD07	PCI_RESV	52
53	+3.3V	PCI_RESV	54
55	PCI_RESV	GND	56
57	PCI_RESV	PCI_RESV	58
59	GND	PCI_RESV	60
61	ACK64	+3.3V	62
63	GND	PCI_RESV	64

Pins for +12V and /BUSMODE2 are not connected to the module. The same applies to JTAG signals TMS and /TRST. JTAG TDI is connected to TDO.

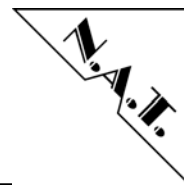


5.7 PMC Connector P13

Table 19: PMC Connector P13

Pin No.	PCI-Signal	PCI-Signal	Pin No.
1	PCI_RESV	GND	2
3	GND	/CBE7	4
5	/CBE6	/CBE5	6
7	/CBE4	GND	8
9	V (I/O)	PAR64	10
11	AD63	AD62	12
13	AD61	GND	14
15	GND	AD60	16
17	AD59	AD58	18
19	AD57	GND	20
21	V (I/O)	AD56	22
23	AD55	AD54	24
25	AD53	GND	26
27	GND	AD52	28
29	AD51	AD50	30
31	AD49	GND	32
33	GND	AD48	34
35	AD47	AD46	36
37	AD45	GND	38
39	V (I/O)	AD44	40
41	AD43	AD42	42
43	AD41	GND	44
45	GND	AD40	46
47	AD39	AD38	48
49	AD37	GND	50
51	GND	AD36	52
53	AD35	AD34	54
55	AD33	GND	56
57	V (I/O)	AD32	58
59	PCI_RESV	PCI_RESV	60
61	PCI_RESV	GND	62
63	GND	PCI_RESV	64

Pins for V(I/O) are not connected to the module. The PCI interface is of 3.3V type, but 5V tolerant.

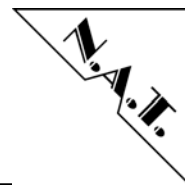


5.8 Pin Assignment of the PMC Connector P14 (PMC I/O)

Table 20: PMC Connector P14

ext. Signal	Pin No.	PCI-Signal	PCI-Signal	Pin No.	ext. Signal
MC	1	I/O	I/O	2	CT_D15
CT_D14	3	I/O	I/O	4	CT_D13
CT_D12	5	I/O	I/O	6	GND
CT_D11	7	I/O	I/O	8	CT_D10
CT_D09	9	I/O	I/O	10	CT_D8
CT_D07	11	I/O	I/O	12	GND
CT_D06	13	I/O	I/O	14	CT_D5
CT_D04	15	I/O	I/O	16	CT_D3
CT_D02	17	I/O	I/O	18	CT_D1
GND	19	I/O	I/O	20	CT_D0
CLKFAIL	21	I/O	I/O	22	/FSYNC
SREF_8K	23	I/O	I/O	24	SCLK
GND	25	I/O	I/O	26	/SCLKx2
SL_4	27	I/O	I/O	28	/C16+
SL_2	29	I/O	I/O	30	SL_3
SL_0	31	I/O	I/O	32	SL_1
SPICK	33	I/O	I/O	34	/SPISEL
SPIMISO	35	I/O	I/O	36	SPIMOSI
/C16-	37	I/O	I/O	38	CT_FRAME_B
CT_FRAME_A	39	I/O	I/O	40	CT_NETREF2
CT_NETREF1	41	I/O	I/O	42	/C4
C2	43	I/O	I/O	44	GND
CT_C8_B	45	I/O	I/O	46	CT_C8_A
CT_D16	47	I/O	I/O	48	CT_D17
CT_D18	49	I/O	I/O	50	CT_D19
GND	51	I/O	I/O	52	CT_D20
CT_D21	53	I/O	I/O	54	CT_D22
CT_D23	55	I/O	I/O	56	CT_D24
GND	57	I/O	I/O	58	CT_D25
CT_D26	59	I/O	I/O	60	CT_D27
CT_D28	61	I/O	I/O	62	CT_D29
CT_D30	63	I/O	I/O	64	CT_D31

The SCbus implemented on the NPMC-8260-E1/T1 is a sub-set of the H.110 bus. SCbus data lines correspond to H.110 data lines CT_D0 – 15.



5.9 The Front Panel Connectors (S1 – S4)

The front panel connectors are 8-pin RJ45 connectors. The 4 E1/T1 line interfaces are available on the pins of the front panel connectors S1 and S2. Table 21: and Table 22: show the pin assignments.

Table 21: Pin Assignment of the Front-panel Connectors S1 (ISDN)

Pin No.	Signal	Signal	Pin No.
1	TX3+	TX3-	2
3	TX1+	RX1+	4
5	RX1-	TX1-	6
7	RX3+	RX3-	8

Table 22: Pin Assignment of the Front-panel Connectors S2 (ISDN)

Pin No.	Signal	Signal	Pin No.
1	TX4+	TX4-	2
3	TX2+	RX2+	4
5	RX2-	TX2-	6
7	RX4+	RX4-	8

Table 23: shows the pin assignment of RJ45-connector S3. This connector carries either the 100BaseT signals of the Ethernet interface, or the signals of the RS232 interface. Which is the actual interface is chosen by an assembly option.

Table 23: Pin Assignment of the Front-panel Connectors S3 (Ethernet)

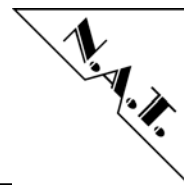
Pin No.	Signal	Signal	Pin No.
1	TX+	TX-	2
3	RX+	Term.	4
5	Term.	RX-	6
7	Term.	Term.	8

Term. is the 100BaseT termination used for pins 4, 5, 7, and 8.

Table 24: shows the pin assignment of the signals of the RS232 interface

Table 24: Pin Assignment of the Front-panel Connectors S4 (RS232)

Pin No.	Signal	Signal	Pin No.
1	not used	RxD_SCC1	2
3	TxD_SCC1	not used	4
5	GND		



6 NPMC-8260-4E1 Programming Notes

6.1 CPU-Setup

The basic setting of the clocks is done by pulling the MODCK pins during /HRESET. These are programmable through CPLD U13 (BA0-2). There are additional 4 bits (MODCK_H) responsible for setting the PLLs, which are read from the Hard Reset Configuration Word. The following RESET – behaviour is performed through hardware:

The chosen PLL setting is MODCK1-3 = 100b for a 166/133/66 MHz CPU version, and MODCK1-3 = 111b for a 200/166/66 MHz. /RSTCONF is tied to GND, therefore the MPC8260 is the configuration master, i.e. it reads configuration data during the /HRESET - phase from FLASH.

Slave configuration is used with the PowerSpan II (PB_RSTCONF is tied to PB_A6).

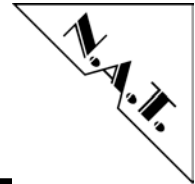
6.2 Hard Reset Configuration Word

In case an empty FLASH shall be programmed via the PCI bus, the MPC8260 can be put into Core Disabled mode by installing a jumper (JP3). This special setting disables the FLASH during configuration read and provides the configuration data through a CPLD.

Table 25: Hard Reset Configuration Word (if read from CPLD)

Bit	Name	Value	Description
0	EARB	0b	internal arbiter active
1	EXMC	0b	internal Memory-Controller
2	CDIS	1b	Core disabled
3	EBM	1b	601 compatible bus mode
4-5	BPS	0b	Boot Port Size 64 bit
6	CIP	1b	Position of the Vector Table is 0H
7	ISPS	0b	64-bit slave
8-9	L2CPC	10b	L2 Cache pins defined as BADDRx
10-11	DPPC	0b	Data Parity Pins used as IRQ pins
12	rsvd	0b	clear
13-15	ISB	010b	initial internal space base select is 0x0F00.0000
16	BMS	1b	boot from low mem
17	BBD	0b	ABB, DBB Pins defined
18-19	MMR	10b	core requests and external master requests 2 & 3 masked
20-21	LBPC	0b	local bus pins enabled
22-23	APPC	10b	Bank Select function selected
24-25	CS10PC	01b	BCTL1 selected
26-27	rsvd	0b	clear
28-31	MODCK_H	0b	PLL configuration, together with MODCK1-3 pins

The **Hard Reset Configuration Word**, which has to be written to FLASH during programming, should contain a similar setting.



6.3 Recommended General Control Register Setup

6.3.1 Register-Setup of the System Clock Control Register (SCCR)

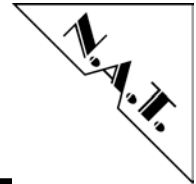
SCCR Bit	Name	Value	Description
Bit 0-28	rsvd	0b	clear
Bit 29	CLPD	0b	CPM does not enter low power mode
Bit 30-31	DFBRG	0b	division factor of 4

6.3.2 Register-Setup of the System Protection Control Register (SYPCR)

SYPCR Bit	Name	Value	Description
Bit 0-15	SWTC	0xFFFF	software watchdog timer count
Bit 16-23	BMT	0xFF	bus monitor timing
Bit 24	PBME	1b	60x bus monitor enabled
Bit 25	LBME	1b	local bus monitor enabled
Bit 26-28	rsvd	0b	clear
Bit 29	SWE	0b	software watchdog disabled
Bit 30	SWRI	1b	watchdog and bus monitors cause soft reset
Bit 31	SWP	1b	software watchdog timer is prescaled

6.3.3 Register-Setup of the Bus Configurations Register (BCR)

BCR Bit	Name	Value	Description
Bit 0	EBM	1b	external bus mode 60x mode
Bit 1-3	APD	100b	address phase delay
Bit 4	L2C	0b	no secondary cache
Bit 5-7	L2D	0b	hit delay, not applicable
Bit 8	PLDP	1b	pipeline max. depth
Bit 9-10	rsvd	0b	clear
Bit 11	EAV	1b	full address on 60x bus
Bit 12	ETM	0b	compatibility mode enable, disabled
Bit 13	LETM	0b	local compatibility mode enable, disabled
Bit 14	EPAR	0b	even parity
Bit 15	LEPAR	0b	local even parity
Bit 16-18	NPQM	111b	non PowerQUICC master
Bit 19-20	rsvd	0b	clear
Bit 21	EXDD	0b	external master delay enabled
Bit 22-26	rsvd	0b	clear
Bit 27	ISPS	0b	internal space port size is 64 bit
Bit 28-31	rsvd	0b	clear



6.3.4 Register-Setup of the 60x Bus Arbiter Configurations Register (PPC_ACR)

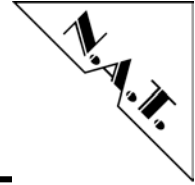
P_ACR Bit	Name	Value	Description
Bit 0-1	rsvd	0b	clear
Bit 2	DBGD	0b	DBG asserted with TS
Bit 3	EARB	0b	internal bus arbitration
Bit 4-7	PRKM	0010b	parking master is CPM low request level

6.3.5 Register-Setup of the Local Bus Arbiter Configurations Register (LCL_ACR)

L_ACR Bit	Name	Value	Description
Bit 0	rsvd	0b	clear
Bit 2	DBGD	0b	DBG asserted with TS
Bit 3	EARB	0b	internal bus arbitration
Bit 4-7	PRKM	0110b	parking master is internal core

6.3.6 Register-Setup of the SIU Module Configurations Register (SIUMCR)

SIUMCR Bit	Name	Value	Description
Bit 0	BBD	0b	ABB, DBB selected
Bit 1	ESE	0b	IRQ1 selected
Bit 2	PBSE	0b	parity byte select disabled
Bit 3	CDIS	0b	core enabled
Bit 4-5	DPPC	00b	IRQ function selected
Bit 6-7	L2CPC	10b	BADDRx selected
Bit 8-9	LBPC	0b	local bus pins selected
Bit 10-11	APPC	10b	BNKSEL function enabled
Bit 12-13	CS10PC	01b	BCTL1 selected
Bit 14-15	BCTLC	0b	buffer control
Bit 16-17	MMR	0b	no masking of bus requests
Bit 18	LPBSE	0b	local parity disabled
Bit 19-31	rsvd	0b	clear

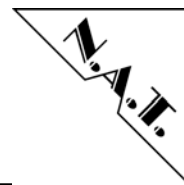


6.3.7 Register-Setup of the 60x Bus Transfer Status/Control Register (TESCR1)

SCCR Bit	Name	Value	Description
Bit 0-16	not used	0b	clear
Bit 17	DMD	1b	all data errors disabled
Bit 18-31	not used	0b	clear

6.3.8 Register-Setup of the Local Bus Transfer Status/Control Register (L_TESCR1)

SCCR Bit	Name	Value	Description
Bit 0-16	not used	0b	clear
Bit 17	DMD	1b	all data parity errors disabled
Bit 18-31	not used	0b	clear



6.4 Recommended Register Setup of the Memory Controller:

6.4.1 Base Registers BRx:

The base addresses given in the description below are the ones chosen for the OK1 and VxWorks implementations for the NPMC-8260-E1/T1. They may be altered to suit the user's needs.

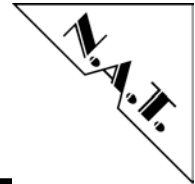
BRx: Base Register of the corresponding CS; CS settings as described in Table 5: above.

BR0 Bit	Name	Value	Description
Bit 0-16	BA	<address>	base address <address>, FLASH
Bit 17-18	rsvd	0b	clear
Bit 19-20	PS	10b	port size 16 bit
Bit 21-22	DECC	0b	ECC disabled
Bit 23	WP	0b	R/W
Bit 24-26	MS	0b	default, 601 bus
Bit 27	EMEMC	0b	memory controller active
Bit 28-29	ATOM	0b	no atomic operations
Bit 30	DR	0b	no data pipelining
Bit 31	V	1b	valid bank

BR1 not used.

BR2 Bit	Name	Value	Description
Bit 0-16	BA	<address>	base address <address>, SDRAM CS0
Bit 17-18	rsvd	0b	clear
Bit 19-20	PS	0b	port size 64 bit
Bit 21-22	DECC	0b	ECC disabled
Bit 23	WP	0b	R/W
Bit 24-26	MS	010b	SDRAM, 601 bus
Bit 27	EMEMC	0b	memory controller active
Bit 28-29	ATOM	0b	no atomic operations
Bit 30	DR	0b	no data pipelining
Bit 31	V	1b	valid bank

The settings of BR2 and BR3 are suitable for the default 32 MB SODIMM module installed. The default module uses only one CS, hence the programming of BR3/OR3 is not necessary.



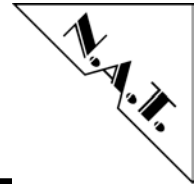
BR3 Bit	Name	Value	Description
Bit 0-16	BA	<address>	base address <address>, SDRAM CS1
Bit 17-18	rsvd	0b	clear
Bit 19-20	PS	0b	port size 64 bit
Bit 21-22	DECC	0b	ECC disabled
Bit 23	WP	0b	R/W
Bit 24-26	MS	010b	SDRAM, 601 bus
Bit 27	EMEMC	0b	memory controller active
Bit 28-29	ATOM	0b	no atomic operations
Bit 30	DR	0b	no data pipelining
Bit 31	V	0b	invalid bank

BR1 not used.

BR5 Bit	Name	Value	Description
Bit 0-16	BA	<address>	base address <address>, TSI
Bit 17-18	rsvd	0b	clear
Bit 19-20	PS	01b	port size 8 bit
Bit 21-22	DECC	0b	ECC disabled
Bit 23	WP	0b	R/W
Bit 24-26	MS	0b	GPCM, 601 bus
Bit 27	EMEMC	0b	memory controller active
Bit 28-29	ATOM	0b	no atomic operations
Bit 30	DR	0b	no data pipelining
Bit 31	V	1b	valid bank

BR6 Bit	Name	Value	Description
Bit 0-16	BA	<address>	base address <address>, QuadFALC
Bit 17-18	rsvd	0b	clear
Bit 19-20	PS	01b	port size 8 bit
Bit 21-22	DECC	0b	ECC disabled
Bit 23	WP	0b	R/W
Bit 24-26	MS	0b	GPCM, 601 bus
Bit 27	EMEMC	0b	memory controller active
Bit 28-29	ATOM	0b	no atomic operations
Bit 30	DR	0b	no data pipelining
Bit 31	V	1b	valid bank

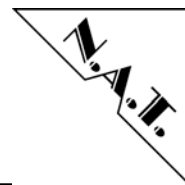
BR7 not used.



BR8 Bit	Name	Value	Description
Bit 0-16	BA	<address>	base address <address>, SRAM (lower half)
Bit 17-18	rsvd	0b	clear
Bit 19-20	PS	11b	port size 32 bit
Bit 21-22	DECC	0b	ECC disabled
Bit 23	WP	0b	R/W
Bit 24-26	MS	001b	GPCM, local bus
Bit 27	EMEMC	0b	memory controller active
Bit 28-29	ATOM	0b	no atomic operations
Bit 30	DR	0b	no data pipelining
Bit 31	V	1b	valid bank

BR9 Bit	Name	Value	Description
Bit 0-16	BA	<address>	base address <address>, SRAM (upper half)
Bit 17-18	rsvd	0b	clear
Bit 19-20	PS	11b	port size 32 bit
Bit 21-22	DECC	0b	ECC disabled
Bit 23	WP	0b	R/W
Bit 24-26	MS	001b	GPCM, local bus
Bit 27	EMEMC	0b	memory controller active
Bit 28-29	ATOM	0b	no atomic operations
Bit 30	DR	0b	no data pipelining
Bit 31	V	1b	valid bank

BR10-11 not used.



6.4.2 Option Registers ORx

The address masks given in the description below are the ones chosen for the OK1 and VxWorks implementations for the NPMC-8260-E1. They may be altered to suit the user's needs.

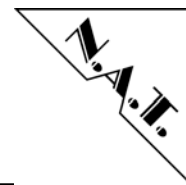
ORx: Option Registers of the corresponding CS, CS settings as described in Table 5: above.

OR0 Bit	Name	Value	Description
Bit 0-16	AM	FF00.0H	address mask, size of the CS range, 16 MB
Bit 17-18	rsvd	0b	clear
Bit 19	BCTLD	0b	BCTLx enabled (R/W control)
Bit 20	CSNT	1b	CS/WE timing parameter
Bit 21-22	ACS	11b	CS timing parameter
Bit 23	rsvd	0b	clear
Bit 24-27	SCY	1011b	11 WS = 13 clock cycles = 170ns access time
Bit 28	SETA	0b	internal TA/PSDVAL generation
Bit 29	TRLX	0b	normal timing
Bit 30	EHTR	0b	normal timing
Bit 31	rsvd	0b	clear

OR1 not used.

OR2 Bit	Name	Value	Description
Bit 0-11	SDAM	FE0H	SDRAM address mask, size of the CS range, 32 MB
Bit 12-16	LSDAM	0H	lower SDRAM address mask
Bit 17-18	BPD	01b	banks per device, default: 4 banks
Bit 19-21	ROWST	0010b	row start address bit (from SDRAM EEPROM), see also DRTYPE _x programming
Bit 22	rsvd	0b	clear
Bit 23-25	NUMR	011b	number of row address lines (from SDRAM EEPROM)
Bit 26	PMSEL	0b	page mode select back to back
Bit 27	IBID	0b	internal bank interleave activated
Bit 28-31	rsvd	0b	clear

The settings of OR2 and OR3 are suitable for the default 32 MB SODIMM module installed. The default module uses only one CS, hence the programming of BR3/OR3 is not necessary.

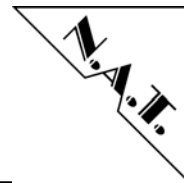


OR3 Bit	Name	Value	Description
Bit 0-11	SDAM	FE0H	SDRAM address mask, size of the CS range, 32 MB
Bit 12-16	LSDAM	0H	lower SDRAM address mask
Bit 17-18	BPD	01b	banks per device, default: 4 banks
Bit 19-21	ROWST	0010b	row start address bit (from SDRAM EEPROM), see also DRYPEx programming
Bit 22	rsvd	0b	clear
Bit 23-25	NUMR	011	number of row address lines (from SDRAM EEPROM)
Bit 26	PMSEL	0b	page mode select back to back
Bit 27	IBID	0b	internal bank interleave activated
Bit 28-31	rsvd	0b	clear

OR4 not used.

OR5 Bit	Name	Value	Description
Bit 0-16	AM	FFFF.0H	address mask, size of the CS range, 64 KB
Bit 17-18	rsvd	0b	clear
Bit 19	BCTLD	0b	L _{WR} enabled (R/W control)
Bit 20	CSNT	0b	CS/WE timing parameter
Bit 21-22	ACS	11b	CS timing parameter
Bit 23	rsvd	0b	clear
Bit 24-27	SCY	0101b	5 WS = 7 clock cycles = 80ns access time
Bit 28	SETA	0b	internal TA/PSDVAL generation
Bit 29	TRLX	1b	relaxed timing
Bit 30	EHTR	1b	extended hold time
Bit 31	rsvd	0b	clear

OR6 Bit	Name	Value	Description
Bit 0-16	AM	FFFF.0H	address mask, size of the CS range, 64 KB
Bit 17-18	rsvd	0b	clear
Bit 19	BCTLD	0b	L _{WR} enabled (R/W control)
Bit 20	CSNT	0b	CS/WE timing parameter
Bit 21-22	ACS	11b	CS timing parameter
Bit 23	rsvd	0b	clear
Bit 24-27	SCY	0101b	5 WS = 7 clock cycles = 80ns access time
Bit 28	SETA	0b	internal TA/PSDVAL generation
Bit 29	TRLX	1b	relaxed timing
Bit 30	EHTR	1b	extended hold time
Bit 31	rsvd	0b	clear



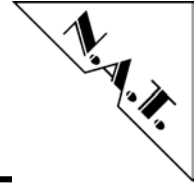
OR7 not used.

OR8 Bit	Name	Value	Description
Bit 0-16	AM	FFFC.0H	address mask, size of the CS range, 256 KB
Bit 17-18	rsvd	0b	clear
Bit 19	BCTLD	0b	L _{WR} enabled (R/W control)
Bit 20	CSNT	0b	C _S /WE timing parameter
Bit 21-22	ACS	11b	CS timing parameter
Bit 23	rsvd	0b	clear
Bit 24-27	SCY	10b	2 WS = 4 clock cycles = 16ns access time
Bit 28	SETA	0b	internal TA/PSDVAL generation
Bit 29	TRLX	0b	normal timing
Bit 30	EHTR	0b	normal timing
Bit 31	rsvd	0b	clear

OR9 Bit	Name	Value	Description
Bit 0-16	AM	FFFC.0H	address mask, size of the CS range, 256 KB
Bit 17-18	rsvd	0b	clear
Bit 19	BCTLD	0b	L _{WR} enabled (R/W control)
Bit 20	CSNT	0b	C _S /WE timing parameter
Bit 21-22	ACS	11b	CS timing parameter
Bit 23	rsvd	0b	clear
Bit 24-27	SCY	10b	2 WS = 4 clock cycles = 16ns access time
Bit 28	SETA	0b	internal TA/PSDVAL generation
Bit 29	TRLX	0b	normal timing
Bit 30	EHTR	0b	normal timing
Bit 31	rsvd	0b	clear

OR8 and OR9 (SRAM) may also be programmed by a free UPM (e.g. UPMB), in order to support bursting. This applies only for MPC8260 versions which support 66 MHz UPM timing.

OR10-11 not used.



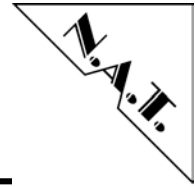
6.4.3 Configuration for SDRAM Register Setup

The correlation between address lines to be multiplexed and the programming of the signals DRTYPE_x and Bank Select (BA_x) is as follows:

DRTYPE_x settings are related to the SODIMM SDRAM row/column organisation. The following table shows which is the highest column address to be multiplexed, which address lines have to be put out by the BA_x lines (BA₀ is not connected), and how SDA₁₀ should be programmed according to the setting of DRTYPE_x:

DRTYPE ₁	DRTYPE ₀	highest col. addr. to be muxed	BA ₁	BA ₂	SDA ₁₀
0	0	SDA ₇	PB_A ₁₉	PB_A ₂₀	PB_A ₈
0	1	SDA ₈	PB_A ₁₈	PB_A ₁₉	PB_A ₇
1	0	SDA ₉	PB_A ₁₇	PB_A ₁₈	PB_A ₆
1	1	SDA ₁₁	PB_A ₁₆	PB_A ₁₇	PB_A ₅

DRTYPE_x are programmable by Port pins of the MPC8260.
 DRTYPE₀ is PD₂₃, DRTYPE₁ is PD₂₂.



6.4.4 SDRAM Mode Register PSDMRx

PSDMR Bit	Name	Value	Description
Bit 0	PBI	1b	page-based Interleave
Bit 1	RFEN	1b	refresh necessary
Bit 2-4	OP	000b	SDRAM operation
Bit 5-7	SDAM	010b	depending on SDRAM parameters and on DRTYPE _x
Bit 8-10	BSMA	110b	depending on SDRAM parameters and on DRTYPE _x
Bit 11-13	SDA10	010b	depending on SDRAM parameters and on DRTYPE _x (see table below)
Bit 14-16	RFRC	110b	depending on SDRAM parameters
Bit 17-19	PRETOACT	100b	depending on SDRAM parameters
Bit 20-22	ACTTORW	100b	depending on SDRAM parameters
Bit 23	BL	0b	burst length is 4
Bit 24-25	LDOTOPRE	10b	depending on SDRAM parameters
Bit 26-27	WRC	11b	depending on SDRAM parameters
Bit 28	EAMUX	1b	external address multiplexer
Bit 29	BUFCMD	0b	normal timing
Bit 30-31	CL	10b	depending on SDRAM parameters

6.4.5 PSRT 60x Bus-Assigned SDRAM Refresh Timer Register

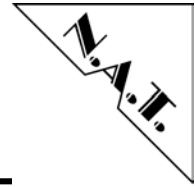
PSRT Bit	Name	Value	Description
Bit 0-7	PSRT	20H	timer value of 32 for prescaler 64

6.4.6 MPTPR Memory Refresh Timer Prescaler Register

MPTPR Bit	Name	Value	Description
Bit 0-7	PSRT	40H	prescaler value 64
Bit 8-15	rsvd	0b	clear

6.4.7 UPM Machine Mode Register MxMR

UPMs are not used in this version. If UPMs are to be used, take the restriction of bus frequency and UPM usage for some MPC8260 masks and versions into account.



6.5 Setup of the Serial Interfaces

6.5.1 RS232 Interface on the Front Panel Connector S4

The programming of the RS232 serial interface is performed through SCC1 (PD30, PD31).

6.5.2 RS232 Debug Interface

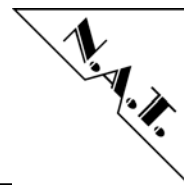
The programming of the RS232 serial debug interface is performed through SMC1 (PD8, PD9).

6.5.3 I²C Interface

The I²C interface is connected to port pins PD14 (Clk) and PD15 (Data). The EEPROM on the SDRAM SODIMM module has address 0 and should be read and analyzed before initialising the SDRAM machine, in order to be able to setup the SDRAM machine, the external logik (DRTYPE_x for U13), and the SDRAMs themselves. The address of the EEPROM U10 used for storage of board-specific parameters is 4. The control code (1st 4 bits of the address) for the 24Cxx EEPROM is 1010b, which results in address \$50 for the SODIMM EEPROM and in address \$54 for the parameter EEPROM.

6.5.4 SPI Interface

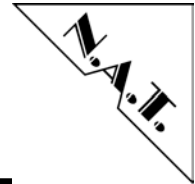
The SPI interface is connected to port pins PD16 (SPIMISO), PD17 (SPIMOSI), PD18 (SPICLK), and PD19 (/SPISEL). It is accessible on the PMC I/O connector P14. No onboard devices are connected to the SPI interface.



6.6 Definition of the Multi-Function Pins

Table 26: Definition of the Multi-Function Pins

Pin Name	Pin Function on the NPMC-8260-E1
DBB/IRQ3	DBB
DP(0-7)/misc.	IRQx
GBL/IRQ1	GBL, not used
CI/BADDR29/IRQ2	BADDR29
WT/BADDR30/IRQ3	BADDR30
L2_HIT/IRQ4	L2_HIT, not used
CPU_BG/BADDR31/IRQ5	BADDR31
CS10/BCTL1/DBG_DIS	BCTL1
CS11/AP0	NC
PWE(0-7)/PSDDQM(0-7)/PBS(0-7)	PSDDQM(0-7)
PSDA10/PGPL0	PSDA10
PSDWE/PGPL1	PSDWE
POE/PSDRAS/PGPL2	PSDRAS
PSDCAS/PGPL3	PSDCAS
PGTA/PUPMWAIT/PGPL4/PPBS	PGTA
PSDAMUX/PGPL5	PSDAMUX
LWE(0-3)/LSDDQM(0-3)/LBS(0-3)	LBS(0-3)
LSDA10/LGPL0	LGPL0, not used
LSDWE/LGPL1	LGPL1, not used
LOE/LSDRAS/LGPL2	LOE
LSDCAS/LGPL3	LGPL3, not used
LGTA/LUPWAIT/LGPL4/LPBS	LGTA
LSDAMUX/LGPL5	LGPL5, not used
L_A15/SMI	L_A15
L_A17/CHKSTO_OUT	L_A17
L_A27/CLKOUT	L_A27
L_A28/CORE_SRESET	L_A28
L_A31/DLLSYNC	L_A31
L_CLDP(0-3)	L_CLDP(0-3), not used
IRQ0/NMIOUT	IRQ0
IRQ7/INTOUT/APE	INTOUT, not used
MODCKx/ApX/TCx/BNKSELx	BNKSELx



6.7 PowerSpan Programming

The PowerSpan II, which bridges between the MPC8260 60x bus (PBus) and the PCI Bus, is initialized by two ways: Power-Up configuration and EEPROM load of setup information on various Reset conditions.

6.7.1 Power-Up Configuration

The Power-Up configuration is loaded by slave configuration through the PowerQUICC II, which configures slave devices during HRESET active period. The PowerSpan’s RSTCONF input is connected to PBus address line A6; hence the PowerSpan is configured as last (but only) slave device. The PowerQUICC II drives a 32-bit configuration word on the data bus, but the PowerSpan takes setup information only from data lines D0 – 7. This setup byte, together with some dedicated setup pins, initializes the PowerSpan to the following modes:

Table 27: PowerSpan II Power-Up Configuration

Function	initialized to
PCIRST:	input
HRESET:	output
PBus PLL:	fast, 66MHz
PCI arbiter:	disabled
PBus arbiter:	disabled
PCI REQ64:	disabled
Boot select:	boot from PBus
Debug mode:	disabled
PLL bypass:	disabled

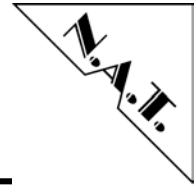
6.7.2 Configuration by EEPROM Load

When reset, the PowerSpan loads several registers from EEPROM, if available. On the NPMC-8260-E1/T1, a 24C02 EEPROM is connected to the I²C interface of the PowerSpan. By default, a long load setup sequence is performed out of this EEPROM. The following data is loaded (please consult the PowerSpan II User’s Manual for a detailed description):

Table 28: PowerSpan II EEPROM Configuration

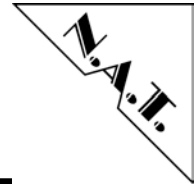
Address	Hex Value
0H	02 00 00 00 00 04 00 A5 5A AB CD 02 18 90 00 00
10H	C0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
20H	82 60 10 E3 06 80 00 01 20 00 40 00 00 02 02 00
30H	00 10 00 00 00 00 00 00 00 00 00 00 00 00 00 00
40H-FFH	FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF

The EEPROM load initializes the PBus Register Space Base Address to 0x1000.0000.



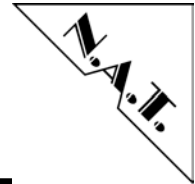
7 Known Bugs

none



Appendix A: Reference Documentation

- [1] Tundra Semiconductor Corp., PowerSpan PCI to Motorola Processor Bridge Manual, April 2002, Document 80A1010_MA001_04
- [2] Motorola Inc., MPC8260 PowerQUICC II User's Manual, 5/1999, Rev.0
- [3] OKI Inc., ML53812-2 Universal Timeslot Interchange, Preliminary Data Sheet, 1996, Rev. 1.3
- [4] Infineon, PEB22554 E1/T1/J1 Framer / Transceiver, 1996, issue 7
- [5] Level One, LXT972A 3.3V Dual-Speed Fast Ethernet Transceiver, 9/2000, Rev. 1.0
- [6] N.A.T. GmbH, NFAPI Manual, 1999, Rev.1.7



Appendix B: Document's History

Revision	Date	Description	Author
	19.01.2001	initial revision	ga
	01.02.2001	layout adaptions	as
1.0	13.07.2001	corrections	ga
1.1	04.09.2001	adaptions to V1.1 hardware	ga
1.2	26.09.2001	amendments to block diagram schematics	ga
	28.09.2001	chapter 7 added	ga
1.3	31.10.2001	additions and amendments in all chapters	ga
1.4	20.12.2001	layout adaptions, amendments to chapter 7	ga
1.5	22.01.2002	adaptions to V1.2 hardware	ga
1.6	22.04.2002	exchanged chapters 3 and 4, chapter 3.1 and 3.2 added, corrections on several pages	ga
1.7	29.05.2002	power consumption data corrected	ga
1.8	27.08.2002	adaptions to V1.3 hardware	ga
1.9	08.10.2002	figure 7 corrected	ga
1.10	08.04.2003	minor corrections	ga
1.11	05.09.2003	figure 7 corrected	ga
1.12	10.09.2003	front panel and LED description added	ga
1.13	02.07.2004	adaptions to V1.4 hardware	ga
1.14	06.08.2004	description of TDM structure reworked	ga
1.15	04.10.2004	adaptions to V1.5 hardware	ga