



NPMC-STM1

Hardware Reference Manual

Version 1.4



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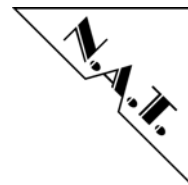
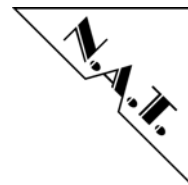


Table of Contents

1	CONVENTIONS	6
1.1	ABBREVIATIONS:	6
2	INTRODUCTION	7
2.1	NPMC-STM1 ORDER CODES.....	9
2.2	SAFETY NOTE	10
2.3	STATEMENT ON ENVIRONMENTAL PROTECTION	10
2.3.1	<i>Compliance to RoHS Directive</i>	<i>10</i>
2.3.2	<i>Compliance to WEEE Directive</i>	<i>11</i>
2.3.3	<i>Compliance to CE Directive</i>	<i>11</i>
2.3.4	<i>Product Safety.....</i>	<i>11</i>
3	HARDWARE OVERVIEW	12
3.1	OPTICAL INTERFACE.....	12
3.2	VT/TU ACCESS	12
3.3	T1/J1/E1 ACCESS	13
3.4	H.110 INTERFACE.....	13
3.5	BACKPLANE TDM ACCESS	13
3.6	PCI-INTERFACE	13
4	HARDWARE DESCRIPTION	14
4.1	PCI INTERFACE	14
4.2	STM1/OC-3 INTERFACE.....	15
4.3	AUTOMATIC PROTECTION SWITCHING (APS) SUPPORT.....	15
5	MEMORY MAP	16
5.1	BOARD CONFIGURATION AND STATUS REGISTERS	16
5.1.1	<i>Register Overview</i>	<i>16</i>
5.1.2	<i>MISC – Misc Control and Status Register</i>	<i>17</i>
5.1.3	<i>Version Register</i>	<i>17</i>
5.1.4	<i>IRQ_Mask – Interrupt Mask Register</i>	<i>18</i>
5.1.5	<i>IRQ_Stat – Interrupt Status Register.....</i>	<i>18</i>
5.1.6	<i>PLL Control and Status Register.....</i>	<i>19</i>
5.1.7	<i>LED-Control Register</i>	<i>19</i>
5.2	MVIP MULTIPLEXER.....	21
6	CONNECTORS.....	22
6.1	PMC CONNECTOR P11	22
6.2	PMC CONNECTOR P12	23
6.3	PMC CONNECTOR P13 (PTMC OPTION H.110).....	24
6.4	PMC CONNECTOR P14 (PMC I/O).....	25
APPENDIX A: REFERENCE DOCUMENTATION.....		26
APPENDIX B: DOCUMENT’S HISTORY.....		27

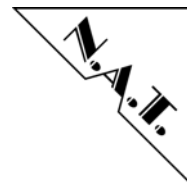


List of Figures

Figure 1: Location Diagram	12
Figure 2: Block Diagram NPMC-STM1	14

List of Tables

Table 1: NPMC-STM1 Technical Data.....	8
Table 2: NPMC-STM1 Order Codes.....	9
Table 3: The Memory Map.....	16
Table 4: FPGA Registers.....	16
Table 5: MISC Control Register.....	17
Table 6: MISC Register Bits	17
Table 7: Version Register	17
Table 8: IRQ_Mask Register.....	18
Table 9: IRQ_Stat Register	18
Table 10: IRQ_Stat Register Bits	18
Table 11: PLL_CSR Register	19
Table 12: PLL_CSR - Register Bits	19
Table 13: LED Control Register.....	19
Table 14: MVIP FPGA Register	21
Table 15: PMC Connector P11.....	22
Table 16: PMC Connector P12.....	23
Table 17: PMC Connector P13.....	24
Table 18: PMC Connector P14.....	25



1 Conventions

If not otherwise specified, addresses and memory maps are written in hexadecimal notation, identified by a prefix *0x* (i.e. *0x1234*).

1.1 Abbreviations:

Abbreviation	Description
b	bit
B	byte
CPU	Central Processing Unit
DMA	Direct Memory Access
DRAM	Dynamic RAM
E1	2.048 Mbit G.703 Interface
Flash	Programmable ROM
K	kilo (factor 400 in hex, factor 1024 in decimal)
M	mega (factor 100000 in hex, factor 1,048,576 in decimal)
MHz	1,000,000 Herz
RAM	Random Access Memory
ROM	Read Only Memory
RTC	Real Time Clock
SRAM	Static RAM
T1	1.544 Mbit G.703 Interface
SC-Bus	Time-Slot Interchange Bus of the SCSA
SCC	Serial Communication Channel of the MPC860
SCSA	Signal Computing System Architecture



2 Introduction

The NPMC-STM1 is a highly optimized PMC module targeting at STM1/SDH and SONET applications. Equipped with a very efficient SDH-to-TDM cross mapping functionality the NPMC-STM1 allows add/drop of all 63 E1 or 84 T1 payloads contained in an VC4 container of an STM-1 frame. The NPMC-STM1 provides this functionality on a single PMC formfactor.

General features:

- Dual Optical Interface for STM1/OC3 at 155Mbit/sec
- Add/Drop Multiplexer for 63E1/84T1 Channels
- H.110-Bus Interface on PMC P14 connector and P13 (PTMC Option)
- 63 E1 Framers or 84 T1 Framers
- Multiplexer cross connect between STM1 E1/T1 payload timeslots and H.110 timeslots
- PCI 2.1 standard compliant bus interface

Features of the Line Interface Circuits:

- Clock recovery and jitter attenuation
- Line and path performance monitoring

Features of the Universal Timeslot Interchange (H.110) circuit:

- Flexible routing of any time slot between each of the framers and the H.110 backplane
- Generation of Clock master signals
- Support of 8 MHz bus clock

Features of the PCI Interface:

- 32 Bit, 33MHz PCI target interface
- 16 bit data, 16 bit address local bus interface
- PCI interrupt support
- Requires only 128 Kbyte address window in PCI memory space

Options:

- Single or Dual Optical Interface
- Single – or Multi-Mode optical Transceiver
- Monitoring Version (dual add/drop multiplexer) for concurrent Rx/Tx monitoring

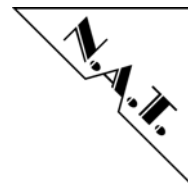
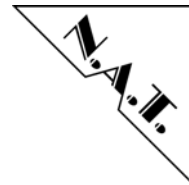


Table 1: NPMC-STM1 Technical Data

PMC-Module	Standard PCI Mezzanine Card Type 1
PCI to local bus bridge	Altera FPGA EP1K30, 33MHz PCI Clock
STM1 Interface	2 Fiber Optic Interfaces for STM1 / OC3 155 Mbit/sec, front-panel connectors
Add/drop Multiplexer	2 x 63E1 Channels or 2 x 84 T1 channels (* Note)
H.110 / SC-Bus	H.110 Universal timeslot Interchange on PMC-I/O connector
Firmware	n.a.
Power consumption	5.0V: 0.5A 3.3V: 2A (fully equipped)
Environment	
Temperature (operating)	0° C to +50 °C, forced air cooling required
Temperature (storage)	-10 °C to +85°C
Humidity	10 % to 90 % noncondensing
Standards compliance	PCI Rev. 2.1 P1386.1 / Draft 2.0

*) **Note:** Due to a limitation within the Zarlink MT90866 H.110 controller, when operation in T1 mode, only 76 of 84 T1 channels can be routed.

This restriction applies to PCB Version 1.1 only !



2.1 NPMC-STM1 Order Codes

The order codes for NPMC-STM1 are organized according to the following scheme:

NPMC-STM1-I-N-P

Table 2 shows the meanings of the used abbreviations:

Table 2: NPMC-STM1 Order Codes

Abbreviation	Description	Option
I	Optical Interface Type	M=Multi Mode S= Single Mode
N	Number of add/drop Multiplexers	1= Single Temux equipped, second optical interface used as backup 2= Dual Temux equipped (Monitoring Version) (* see Note)
P	PTMC Option	P=PTMC Connector (P13) equipped

*) **Note:** Theoretically this version would be capable of handling 2 x 63E1 or 2 x 84 T1 channels (=4032 timeslots) in full duplex mode (add/drop). But the total amount of timeslots is restricted by the number of timeslots the H.110 backplane bus and the timeslot interface chip (Zarlink MT90866) can handle. Thus the total amount of timeslots is restricted to 4096 (half duplex).



2.2 Safety Note

Electrostatic discharge and incorrect board installation and removal can damage the circuitry or shorten its service life.

To ensure proper operation of the **NPMC-STM1** during its usual lifetime take the following precautions before handling the board.

- Before installing or deinstalling the **NPMC-STM1**, read the Installation Guide and the User's Manual for the PMC carrier board
- Before touching integrated circuits, take all the necessary precautions for handling electrostatic devices.
- Ensure that the **NPMC-STM1** is connected to the carrier board with all three PMC connectors properly seated and that the power is available (GND, +5V, and +3.3V).
- When operating the board in areas of strong electromagnetic radiation ensure that the module
 - is screwed to the front panel, VME or cPCI rack and
 - shielded by a closed housing.

2.3 Statement on Environmental Protection

2.3.1 Compliance to RoHS Directive

Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) predicts that all electrical and electronic equipment being put on the European market after June 30th, 2006 must contain lead, mercury, hexavalent chromium, polybrominated biphenyls (PBB) and polybrominated diphenyl ethers (PBDE) and cadmium in maximum concentration values of 0.1% respective 0.01% by weight in homogenous materials only.

As these hazardous substances are currently used with semiconductors, plastics (i.e. semiconductor packages, connectors) and soldering tin any hardware product is affected by the RoHS directive if it does not belong to one of the groups of products exempted from the RoHS directive.

Although many of hardware products of N.A.T. are exempted from the RoHS directive it is a declared policy of N.A.T. to provide all products fully compliant to the RoHS directive as soon as possible. For this purpose since January 31st, 2005 N.A.T. is requesting RoHS compliant deliveries from its suppliers. Special attention and care has been paid to the production cycle, so that wherever and whenever possible RoHS components are used with N.A.T. hardware products already.



2.3.2 Compliance to WEEE Directive

Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) predicts that every manufacturer of electrical and electronic equipment which is put on the European market has to contribute to the reuse, recycling and other forms of recovery of such waste so as to reduce disposal. Moreover this directive refers to the Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS).

Having its main focus on private persons and households using such electrical and electronic equipment the directive also affects business-to-business relationships. The directive is quite restrictive on how such waste of private persons and households has to be handled by the supplier/manufacturer, however, it allows a greater flexibility in business-to-business relationships. This pays tribute to the fact with industrial use electrical and electronic products are commonly integrated into larger and more complex environments or systems that cannot easily be split up again when it comes to their disposal at the end of their life cycles.

As N.A.T. products are solely sold to industrial customers, by special arrangement at time of purchase the customer agreed to take the responsibility for a WEEE compliant disposal of the used N.A.T. product. Moreover, all N.A.T. products are marked according to the directive with a crossed out bin to indicate that these products within the European Community must not be disposed with regular waste.

If you have any questions on the policy of N.A.T. regarding the Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) or the Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) please contact N.A.T. by phone or e-mail.

2.3.3 Compliance to CE Directive

Compliance to the CE directive is declared. A 'CE' sign can be found on the PCB.

2.3.4 Product Safety

The board complies to EN60950 and UL1950.

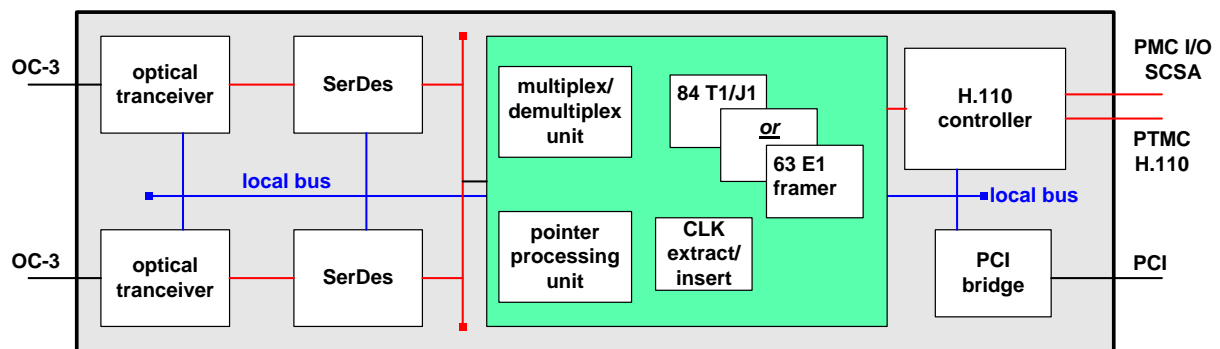


3 Hardware Overview

The NPMC-STM1 is a telecommunications interface board in PMC (PCI mezzanine card) form factor. The NPMC-STM1 is targeted at telecom applications dealing with Synchronous Digital Hierarchy (SDH), such as SS7, ISDN or 3G/3.5G mobile applications in optical OC-3/STM-1 and SONET environments.

Being equipped with an add/drop multiplexer/demultiplexer chipset the NPMC-STM1 is an ideal single board platform to interface between the frame oriented STM-1/SDH networks and classic TDM (*T*ime *D*ivision *M*ultiplex) standards as E1/T1/J1. Possible applications are i.e. add/drop multiplexer or terminal multiplexer.

Figure 1: Location Diagram



3.1 Optical Interface

The two optical 155Mbps OC-3/STM-1 line interfaces are available on two standard OC-3 SDH/STM-1 connectors at the front panel.

3.2 VT/TU Access

The two OC-3/STM1 framers are connected to an add/drop multiplexer/demultiplexer chipset. Since the chip performs the entire SDH pointer processing it is capable of accessing STS-1 SPEs (Synchronous Payload Envelopes), TUG3 tributary unit groups within in VC4 container as well as VC3 virtual containers and thus to extract/insert any of the 84 T1/J1 or 63 E1 streams including the respective clocking information contained in a single STM-1 SDH frame. Supported mappings are VT1.5/VT-2 to STS-1 SPE, TU-11/TU-12 to STM-1/VC3 or to TUG3 to STM-1/VC4.

The chip supports the M13 and G.747 multiplexing.



3.3 T1/J1/E1 Access

The multiplexer/demultiplexer chipset interfaces to 84 T1/J1 framers or 63 E1 timesliced framers, each having individual Rx/Tx, CLK and SYNC signals. For T1 the framing standards SF, SLC-96 and ESF, for E1 G.704 and G.706 (CRC-4 multiframe), for J1 the TTC JT-G.704 as well CRC-6 calculation are supported. The chip also provides full jitter attenuation.

3.4 H.110 Interface

The T1/J1/E1 framers interface to the onboard H.110 controller. The H.110 controller allows flexible 64kbps timeslot routing between the various T1/J1/E1 streams as well as the selection of one of the T1/J1/E1 clocks as the master clock for the TDM backplane bus. Thus it is possible to distribute all 84 T1/J1 or 63 E1 streams jitter-free and synchronised via the backplane.

3.5 Backplane TDM Access

The onboard H.110 bus controller offers access to the backplane TDM bus supporting full the H.110 bus (PTMC) or the SC Bus subset on the PMC multi-purpose I/O connectors.

3.6 PCI-Interface

The NPMC-STM1 is a P1386.1/Draft 2.0 compatible PMC module, that can be plugged onto any VME, cPCI or other carrier board offering a PMC extension slot. The NPMC-STM1 is PCI Rev. 2.2 compatible (32bit).

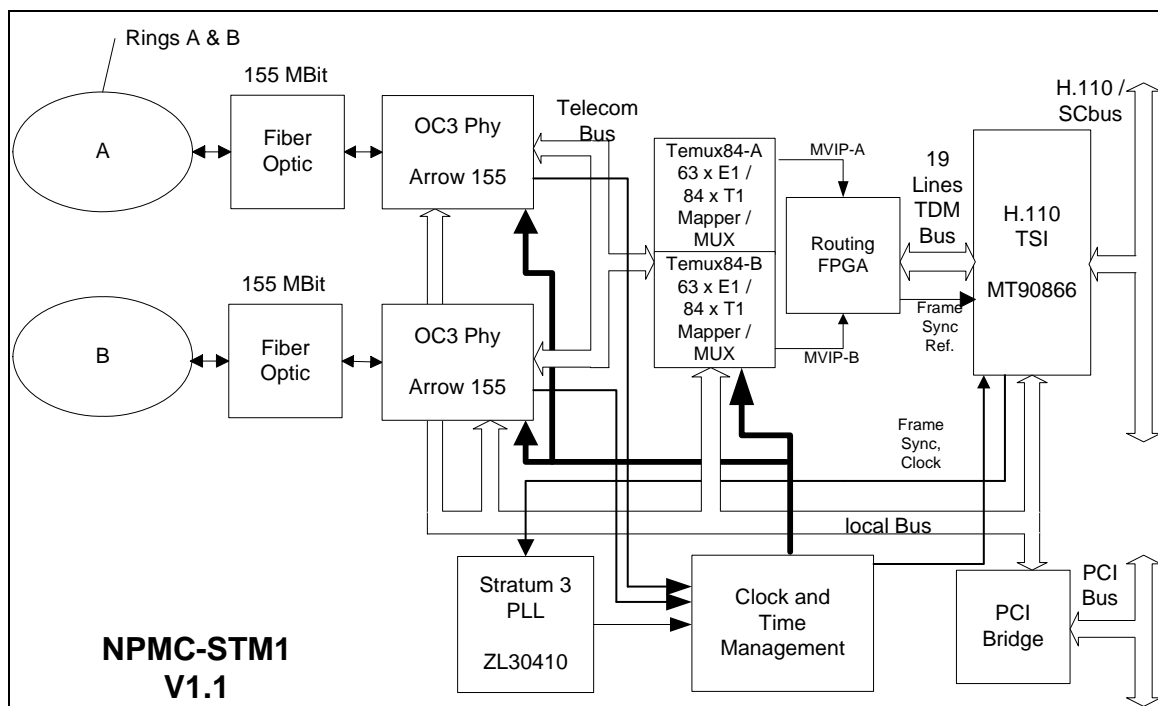


4 Hardware Description

The NPMC-STM1 is a standard form factor PMC module. It has a dual optical interface (OC-3) which is connected via framers (Arrow155) with one or two add/drop Multiplexer devices (Temux84). For standard applications only one Temux is required as the second optical ring acts as a backup ring. For monitoring applications or all applications where direct data access to both optical rings is required, a second add/drop multiplexer can be assembled. On the backplane side the E1 or T1 streams from both Temux chips are merged together into one TDM bus which interfaces to the H.110 timeslot interface chip.

Figure 2 shows a detailed block diagram of the NPMC-STM1.

Figure 2: Block Diagram NPMC-STM1



4.1 PCI Interface

The PCI interface is a standard 32Bit/33MHz target interface contained in a FPGA. The PCI-FPGA also contains a set of registers which control the operation of the NPMC-STM1 Module.



4.2 STM1/OC-3 Interface

The STM1/OC3 interface consists of the Fiber Optic interface and the Sonet/SDH framer. The PMC-Sierra device Arrow-155 as Sonet/SDH framer.

The Arrow-155 is a single port Sonet/SDH framer supporting the OC-3 (STM-1) data rates. The Arrow-155 terminates section, line and path overhead of both the STS-n (AU-4) level and the TU-3 level. On the line side it incorporates a SERDES, allowing it to mate directly to an optics module. The system side interface is an 8-bit multi-drop parallel Telecom bus, allowing multiple devices to share a single bus. The Arrow-155 maps/demaps up to three channels of DS3, E3, or EC-1 with bi-directional monitoring of traffic. The traffic may be multiplexed either into the system side or line side interfaces.

4.3 Automatic Protection Switching (APS) Support

The Arrow-155 extracts and filters the K1/K2 bytes from three frames. The filtered K1/K2 bytes are accessible through the memory mapped registers of the framers. Error conditions detected within in K1/K2 bytes will lead to a device interrupt if not masked.



5 Memory Map

The following table gives a detailed overview of the internal address map of the **NPMC-STM1**. All addresses are given as offsets to the PCI memory space base address. In total the NPMC-STM1 requires a PCI memory window of 128Kbyte.

Table 3: The Memory Map

Address Offset	Device	Access	Comments
0x00000	PCI-FPGA	16 Bit r/w	Board Configuration and Status Registers
0x04000	MVIP-FPGA	8 Bit r/w	MVIP Bus Multiplexer
0x08000	MT90866	16 Bit r/w	H.110 Bus Controller
0x10000	Temux84-A	Even Byte r/w	E1/T1 Framer - Byte interleave Access only -
0x14000	Temux84-B	Even Byte r/w	E1/T1 Framer - Byte interleave Access only -
0x18000	Arrow-155-A	16 Bit r/w	Sonet/SDH Framer – A Ring
0x1c000	Arrow-155-B	16 Bit r/w	Sonet/SDH Framer – B Ring

For a detailed description of the Temux84, MT90866 and Arrow-155 registers, please refer to the respective manuals of these chips.

The board configuration and status registers which are contained in the Altera FPGA are described within the following sections.

5.1 Board Configuration and Status Registers

5.1.1 Register Overview

The following table gives an overview of all registers contained in the Altera FPGA:

Table 4: FPGA Registers

Address	Reset Value	Name	Description
0x00	0x0000	MISC	Misc Control and Status
0x02	0x0000	VER	Version Register
0x04	0x0000	IRQ_Mask	Interrupt Mask Register
0x06	0x0000	IRQ_Stat	Interrupt Status Register
0x08	0x0000	PLL_CSR	PLL Control/Status Register
0x0A	0x1110	LED	Led Control Register



5.1.2 MISC – Misc Control and Status Register

The MISC register contains some general purpose control and status registers

Table 5: MISC Control Register

MISC - Address 0x00																
Default value 0x0000																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Func	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	Reset

Table 6: MISC Register Bits

Bit	Name	Function
0	Reset	Write 1 to initiate a Reset to all onboard devices, reads 0 when the reset is passed by

5.1.3 Version Register

The Version Register shows the actual PCB and FPGA releases.

Table 7: Version Register

LED - Address 0x02																
Default value 0x1110																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Func	PCB Version								FPGA Version							



5.1.4 IRQ_Mask – Interrupt Mask Register

The Interrupt Mask Register allows the individual masking of the interrupt sources. Interrupt sources which are enabled are wired or'ed to the PCI INTA pin, thus leading to an PCI interrupt. The source for the interrupt can be read from the IRQ_Stat register. The meaning of the individual bits is explained in Table 10.

Table 8: IRQ_Mask Register

IRQ_Mask - Address 0x04																
Default value 0x0000																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Func	-	-	-	-	-	-	-	-	-	-	-	-	IRQ4	IRQ3	IRQ2	IRQ1

0 = Interrupt is disabled
 1 = Interrupt is enabled

5.1.5 IRQ_Stat – Interrupt Status Register

By means of the IRQ_Stat register the status of the interrupt lines of the individual onboard interrupt sources can be determined. The value of a bit does not depend on the setting of the corresponding bit in the IRQ_Mask register. If a bit in the IRQ_Stat register is set and the corresponding bit in the IRQ_Mask register is enabled, the PCI interrupt line INTA will be activated.

The following table shows the assignment of the register bits.

Table 9: IRQ_Stat Register

IRQ_Stat - Address 0x06																
Default value 0x0000																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Func	-	-	-	-	-	-	-	-	-	-	-	-	IRQ4	IRQ3	IRQ2	IRQ1

Table 10: IRQ_Stat Register Bits

Bit	Name	Function
0	IRQ1	Arrow-A interrupt active
1	IRQ2	Arrow-B interrupt active
2	IRQ3	Temux-84-A interrupt active
3	IRQ4	Temux-84-B interrupt active



5.1.6 PLL Control and Status Register

The PLL Control Register configures the main 77.76Mhz Telecom clock configuration. The status of the PLL can be read on the upper half of the register.

Table 11: PLL_CSR Register

Clk_Cntr - Address 0x08																
Default value 0x0000																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Func	-	-	-		Secor	Prior	Hold Over	Lock	-	-	-	-	PLL_Mode	CLK77_REF		

Table 12: PLL_CSR - Register Bits

Bit	Name	Function
[1..0]	CLK77_REF	Reference select for the 77.6 MHz Telecom Bus Clock 0x0 – 77.6 MHz Crystal Oszillator – free running 0x1 – Arrow-A 0x2 – Arrow-B 0x3 – H.110, CLK_A or CLK_B
[3..2]	PLL_Mode	Main PLL Mode Selection 0x0 – Normal Mode 0x1 – Holdover Mode 0x2 – Free running Mode 0x3 – reserved
8	Lock	PLL is locked to primary or secondary reference clock
9	Hold Over	PLL is in transition state (lock not yet achieved)
10	Prior	Primary clock out of lock m(see Note*)
11	Secor	Secondary clock out of lock (see Note*)

*) **Note:** The primary clock selection is made by bits CLK77_REF, the secondary clock input is not used.

5.1.7 LED-Control Register

The LED-Control Register is used to switch on/off the 8 front panel leds.

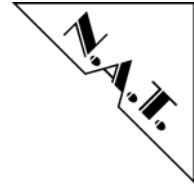
Table 13: LED Control Register

LED - Address 0x0A																
Default value 0x0000																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W



Func	-	-	-	-	-	-	-	-	Led8	Led7	Led6	Led5	Led4	Led3	Led2	Led1
------	---	---	---	---	---	---	---	---	------	------	------	------	------	------	------	------

1 = Led is on
0 = Led is off



5.2 MVIP Multiplexer

The MVIP multiplexer connects the MVIP system busses of the two Temux84 devices to the Zarlink H.110 controller.

The MVIP multiplexer enables the individual connection of each of the 21 MVIP ports of the Temux-A and Temux-B with the 19 ports of the Zarlink H.110 controller.

When the system is operating in E1 mode all used ports of one Temux (18 ports) can be mapped to the H.110 controller or a mixture of ports from both Temux allowing in total 19 MVIP ports to be connected.

When operating in T1 mode only 19 of the 21 lines from the Temux can be mapped due to the limitation within the Zarlink chip. This means that in T1 mode not the full bandwidth of a 155MBit OC3 line can be dropped or added. *This restriction applies to PCB Version V1.1 only!*

The MVIP multiplexer is realized within an Altera FPGA. The FPGA consists of 19 registers which are assigned to the 19 available ports of the Zarlink H.110 controller. The value written into one of the registers selects a port from one of the Temux chips and connects it to the port of the H.110 controller which is defined by the register number.

The following table shows the FPGA register layout and bit meanings.

Table 14: MVIP FPGA Register

MVIP - Address 0x4000 – 4024																
Default value 0x0000																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Func	-	-	-	-	-	-	-	-	-	-	Temux Dev	Temux Port				

Temux Dev = [1..0] = Selection between Temux-A and Temux –B

Temux Port = [20..0] = Port to be connected from selected Temux



6 Connectors

6.1 PMC Connector P11

Table 15: PMC Connector P11

Pin	No.	PCI-Signal	PCI-Signal	Pin No.
1		TCK	-12V	2
3		GND	/INT A	4
5		/INT B	/INT C	6
7		/BUSMODE1	+5V	8
9		/INT D	PCI_RSV1	10
11		GND	3.3Vaux	12
13		CLK	GND	14
15		GND	/GNT	16
17		/REQ	+5V	18
19		V (I/O)	AD31	20
21		AD28	AD22	22
23		AD25	GND	24
25		GND	CBE3	26
27		AD22	AD21	28
29		AD19	+5V	30
31		V (I/O)	AD17	32
33		/FRAME	GND	34
35		GND	/IRDY	36
37		/DEVSEL	+5V	38
39		GND	/LOCK	40
41		/SDONE	/SBO	42
43		PAR	GND	44
45		V (I/O)	AD15	46
47		AD12	AD11	48
49		AD09	+5V	50
51		GND	/CBE0	52
53		AD06	AD05	54
55		AD04	GND	56
57		V (I/O)	AD03	58
59		AD02	AD01	60
61		AD00	+5V	62
63		GND	/REQ64	64

Pins for –12V, Vaux, and V(I/O) are not connected to the module. The same applies to JTAG signal TCK and PCI signals /LOCK, /SDONE, /SBO, /INTB, /INTC, /INTD. The PCI bridge chip always drives signals to 3.3V level, but it 5V tolerant.

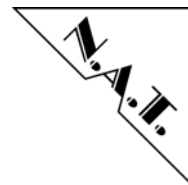


6.2 PMC Connector P12

Table 16: PMC Connector P12

Pin	No.	PCI-Signal	PCI-Signal	Pin No.
1		+12V	/TRST	2
3		TMS	TDO	4
5		TDI	GND	6
7		GND	PCI_RS3V3	8
9		PCI_RS3V3	PCI_RS3V4	10
11		/BUSMODE2	+3.3V	12
13		/PCIRST	/BUSMODE3	14
15		+3.3V	/BUSMODE4	16
17		/PME	GND	18
19		AD30	AD29	20
21		GND	AD26	22
23		AD24	+3.3V	24
25		IDSEL	AD23	26
27		+3.3V	AD20	28
29		AD18	GND	30
31		AD16	/CBE2	32
33		GND	PCI_RESVD	34
35		/TRDY	+3.3V	36
37		GND	/STOP	38
39		/PERR	GND	40
41		+3.3V	/SERR	42
43		/CBE1	GND	44
45		AD14	AD13	46
47		M66EN	AD10	48
49		AD08	+3.3V	50
51		AD07	PCI_RESV	52
53		+3.3V	PCI_RESV	54
55		PCI_RESV	GND	56
57		PCI_RESV	PCI_RESV	58
59		GND	PCI_RESV	60
61		ACK64	+3.3V	62
63		GND	PCI_RESV	64

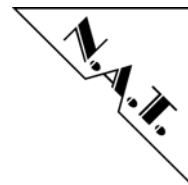
Pins for +12V and /BUSMODE2 are not connected to the module. The same applies to JTAG signals TMS and /TRST. JTAG TDI is connected to TDO.



6.3 PMC Connector P13 (PTMC Option H.110)

Table 17: PMC Connector P13

ext. Signal	Pin No.	Pin No.	ext. Signal
CT_D26	1	2	GND
GND	3	4	-
CT_D24	5	6	-
CT_D22	7	8	GND
V(I/O)	9	10	CT_D31
GNDZ11	11	12	CT_D29
CT_D20	13	14	GND
GND	15	16	CT_D27
CT_FRAME_A	17	18	CT_D25
CT_FRAME_B	19	20	GND
V(I/O)	21	22	CT_D23
GNDZ23	23	24	CT_D21
CT_C8_A	25	26	GND
GND	27	28	CT_D19
CT_D18	29	30	CT_D17
CT_D16	31	32	GND
GND	33	34	CT_NETR2
CT_D14	35	36	CT_D30
CT_D12	37	38	GND
/PTEN	39	40	CT_D28
GNDZ41	41	42	CT_NETR1
CT_C8_B	43	44	GND
GND	45	46	CT_D15
CT_D10	47	48	CT_D13
CT_D8	49	50	CT_D11
GND	51	52	CT_D9
CT_D7	53	54	CT_D6
CT_D4	55	56	GND
-	57	58	CT_D5
CT_D2	59	60	CT_D3
CT_D1	61	62	GND
GND	63	64	CT_D1



6.4 PMC Connector P14 (PMC I/O)

Table 18: PMC Connector P14

ext.	Signal	Pin No.	Pin No.	ext. Signal
MC		1	2	CT_D15
CT_D14		3	4	CT_D13
CT_D12		5	6	GND
CT_D11		7	8	CT_D10
CT_D09		9	10	CT_D8
CT_D07		11	12	GND
CT_D06		13	14	CT_D5
CT_D04		15	16	CT_D3
CT_D02		17	18	CT_D1
GND		19	20	CT_D0
-		21	22	CT_FRAME_A/ FSYNC
CT_NETR1/ SREF_8K		23	24	CT_C8_A/SCLK
GND		25	26	CT_C8_A
-		27	28	-
-		29	30	-
-		31	32	-
-		33	34	-
-		35	36	-
-		37	38	CT_FRAME_B
CT_FRAME_A		39	40	CT_NETREF2
CT_NETREF1		41	42	-
-		43	44	GND
CT_C8_B		45	46	CT_C8_A
CT_D16		47	48	CT_D17
CT_D18		49	50	CT_D19
GND		51	52	CT_D20
CT_D21		53	54	CT_D22
CT_D23		55	56	CT_D24
GND		57	58	CT_D25
CT_D26		59	60	CT_D27
CT_D28		61	62	CT_D29
CT_D30		63	64	CT_D31

The SCbus implemented on the **NPMC-STM1** is a sub-set of the H.110 bus. SCbus data lines correspond to H.110 data lines CT_D0 – 15.



Appendix A: Reference Documentation

- [1] Zarlink: MT90866 Data Sheet
- [2] PMC Sierra: PM8316 – TEMUX84 Register Description, Issue March 2004
- [3] PMC Sierra: PM8316 – TEMUX84 Programmers Guide, Issue No. 4: Sep. 2003
- [4] PMC Sierra: PM5318/5320 – Arrow622/155 Operation and Configuration Guide
Issue No.2, Jul 2004
- [5] PMC Sierra: PM5318/5320 – Arrow155 Register Description, Issue No.2, Jul 2004



Appendix B: Document's History

Version	Date	Description	Author
1.0	1.7.04	Initial Version	hl
1.1	31.1.2005	Reworked	hl
1.2	29.9.2005	Removed signal CLKFAIL from P14 description	hl
1.3	10.02.2006	'Statement on Environmental Protection' added	ga
1.4	06.06.2007	chapters 2.3.3. and 2.3.4. added	ga