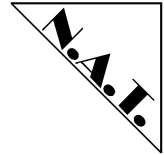


**NPMC-860-4S0
CPU PMC Module
Technical Reference Manual V1.3
HW Revision 2.0**



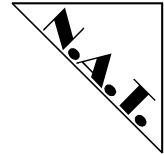
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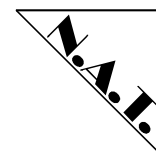
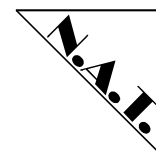


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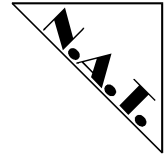
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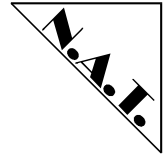
Conventions

If not otherwise specified, addresses and memory maps are written in hexadecimal notation, identified by *0x*.

Table 1 gives a list of the abbreviations used in this document:

Table 1: List of used Abbreviations

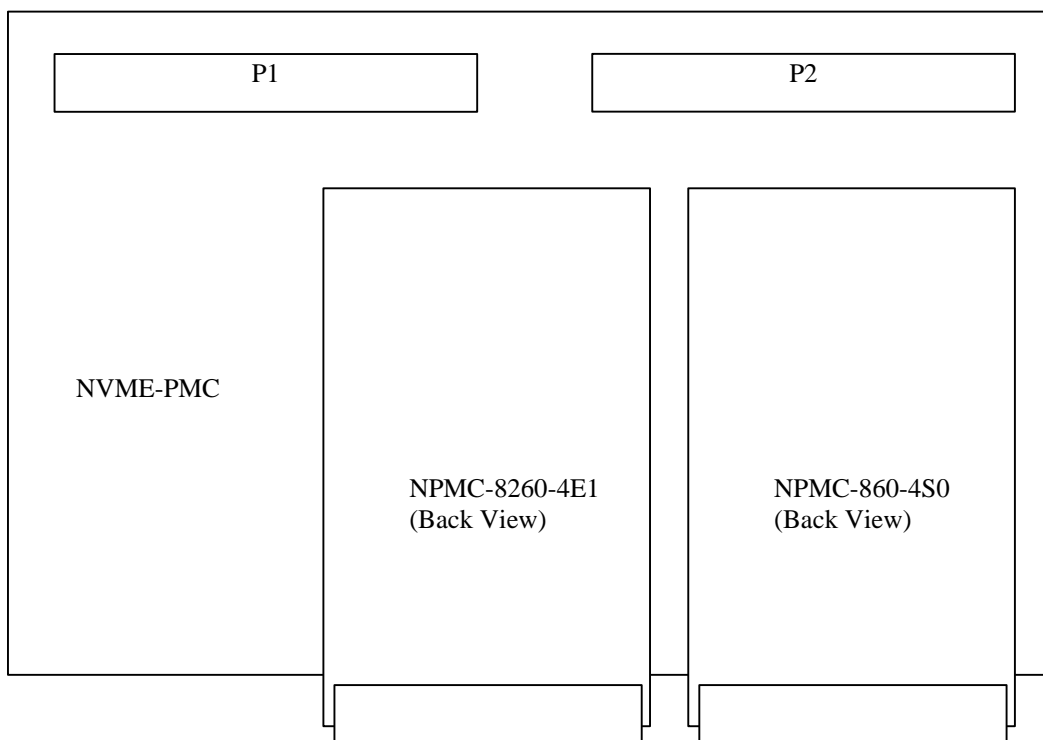
Abbreviation	Description
b	Bit, binary
B	byte
CPU	Central Processing Unit
DMA	Direct Memory Access
Flash	Programmable ROM
H.110	Time-Slot Interchange Bus
ISDN	Integrated Services Digital Network
K	kilo (factor 400 in hex, factor 1024 in decimal)
LIU	Line Interface Unit
M	mega (factor 10,000 in hex, factor 1,048,576 in dec)
MHz	1,000,000 Herz
ML53812	Oki H.110 Controller
MPC860	Embedded processor from Motorola
PowerQUICC	MPC860
Qbus	PowerPC processor bus
QSpan II	Tundra PCI → 60x bus interface device
RAM	Random Access Memory
ROM	Read Only Memory
SCbus	Time-Slot Interchange Bus of the SCSA, subset of H.110 bus
SCC	Serial Communication Controller of the MPC860
SCSA	Signal Computing System Architecture
SDRAM	Synchronous Dynamic RAM
SMC	Serial Communication Controller of the MPC860
SRAM	Static RAM
S/T port	framer and line interface for basic rate ISDN
TDM	Time Division Multiplex
TSA	Time Slot Assigner
TSI	Time Slot Interchange



1 Introduction

The **NPMC-860-4S0** is a high performance standard CPU PCI Mezzanine Card Type 1. It can be plugged onto any carrier board supporting PMC standards:

Figure 1: NPMC-860-4S0 on a VMEbus carrier



The **NPMC-860-4S0** has the following mayor features on-board:

- PowerQUICC MPC860 based Embedded PowerPC Architecture
- Front-panel I/O
- PCI Bus interface
- Single Slot VME/cPCI solution together with the PMC carrier board

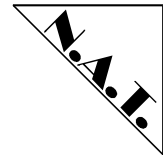
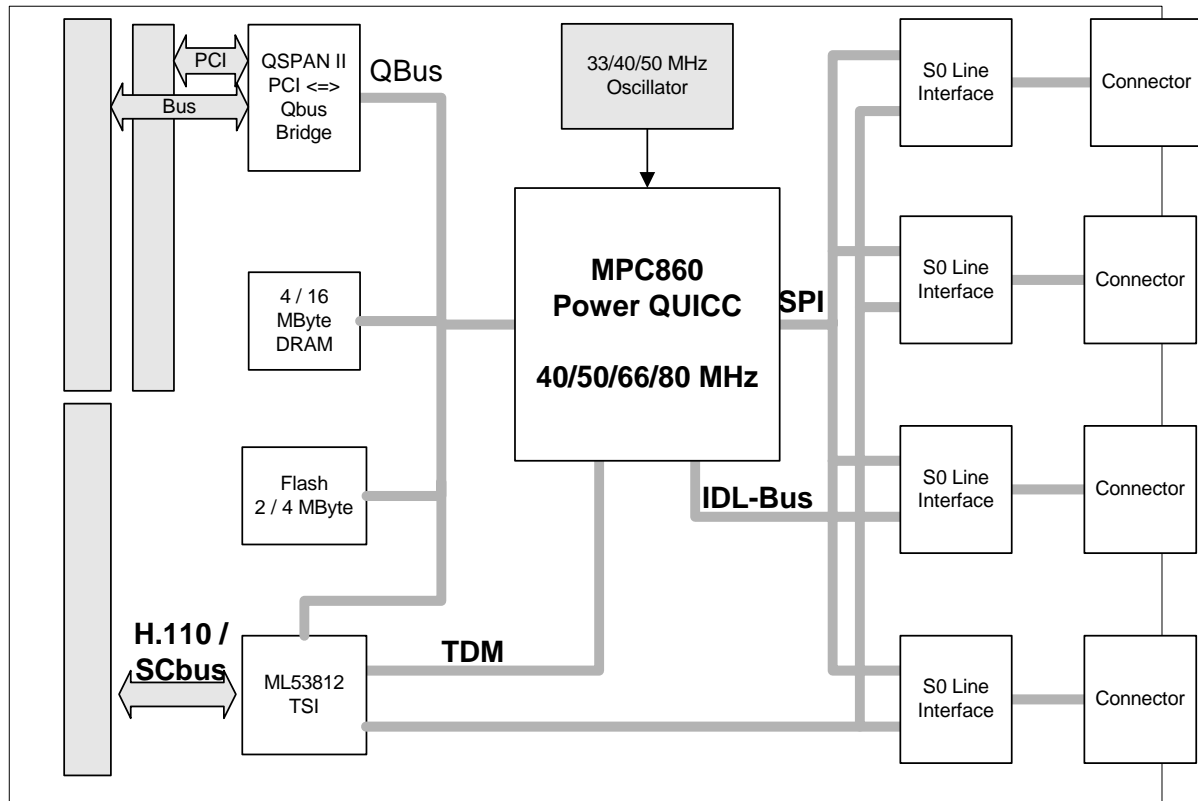


Figure 2: NPMC-860-4S0 Block Diagram



The onboard devices are in detail as follows:

- **Memory**

DRAM: The **NPMC-860-4S0** provides 4 or 16 MByte EDO DRAM onboard. The DRAM is 32 bit wide.

Flash PROM: The 8 bit boot Flash PROM provides a maximum capacity of 4 MByte.

- **Interfaces**

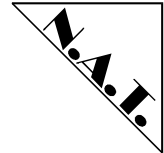
PCI: The **NPMC-860-4S0** includes a 32 bit 33 MHz PCI bus interface.

- **I/O**

The 4 S0 line interfaces are connected to the front panel connectors. The SCbus is connected to the PCI I/O connector.

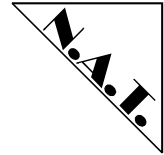
- **CPU**

Depending on the assembled CPU type the PowerQUICC runs with a minimum frequency of 50 MHz. (40 MHz, 66 MHz, or 80 MHz versions are optionally available)



1.1 Specification

Processor	PowerQUICC MPC860
PMC-Module	Standard PCI Mezzanine Card Type 1
PCI to QBUS bridge	QSPAN II
I/O	4 RJ45 connectors
Main Memory	4 / 16 MByte EDO DRAM
Flash PROM	2 / 4 MByte Flash PROM, on-board programmable
Firmware	OK1, PSOS BSP, VxWorks BSP (on request)
Power consumption	3.3V 0,8A 5.0V 0,5A
Environm. conditions Temperature (operating) Temperature (storage) Humidity	0°C to +50°C -40°C to +85°C 5 % to 95 % noncondensing
Standards compliance	PCI Rev. 2.2 P1386.1 / Draft 2.4



2 Installation

2.1 Safety Note

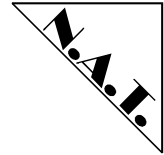
To ensure proper functioning of the **NPMC-860-4S0** during its usual lifetime take the following precautions before handling the board.

CAUTION

Malfunction or damage to the board or connected components

Electrostatic discharge and incorrect board installation and uninstallation can damage circuits or shorten their lifetime.

- Before installing or uninstalling the board read this installation section
- Before installing or uninstalling the **NPMC-860-4S0**, read the Installation Guide and the User's Manual of the **NPMC-860-4S0** carrier board
- Before installing or uninstalling the **NPMC-860-4S0** on a carrier board or both in a VME/cPCI rack:
 - Check all installed boards and modules for steps that you have to take before turning on or off the power.
 - Take those steps.
 - Finally turn on or off the power.
- Before touching integrated circuits ensure to take all require precautions for handling electrostatic devices.
- Ensure that the **NPMC-860-4S0** is connected to the carrier board via all PMC connectors and that the power is available on both PMC connectors (GND, +5V, and +3,3V).
- When operating the board in areas of strong electromagnetic radiation ensure that the module
 - is bolted the front panel or VME/cPCI rack
 - and shielded by closed housing.



2.2 Installation Prerequisites and Requirements

IMPORTANT

Before powering up

- check this section for installation prerequisites and requirements

2.2.1 Requirements

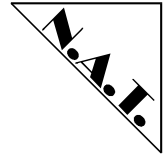
The installation requires only

- a carrier board for connecting the **NPMC-860-4S0**
- power supply

2.2.2 Power supply

The power supply for the **NPMC-860-4S0** must meet the following specifications:

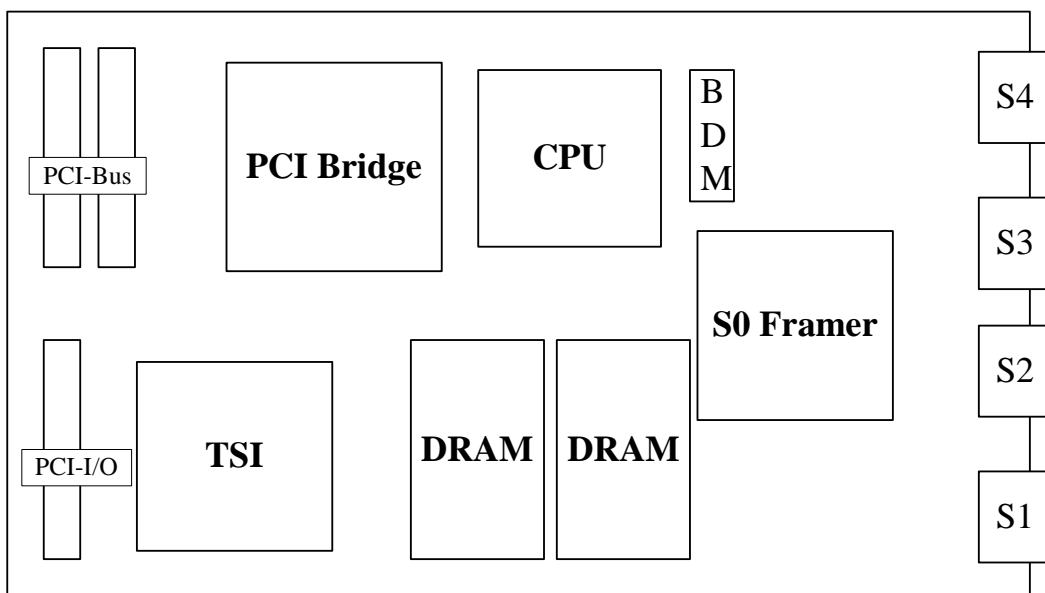
- required for the module:
 - +3,3V / 0,8A typical
 - +5,0V / 0,5A typical



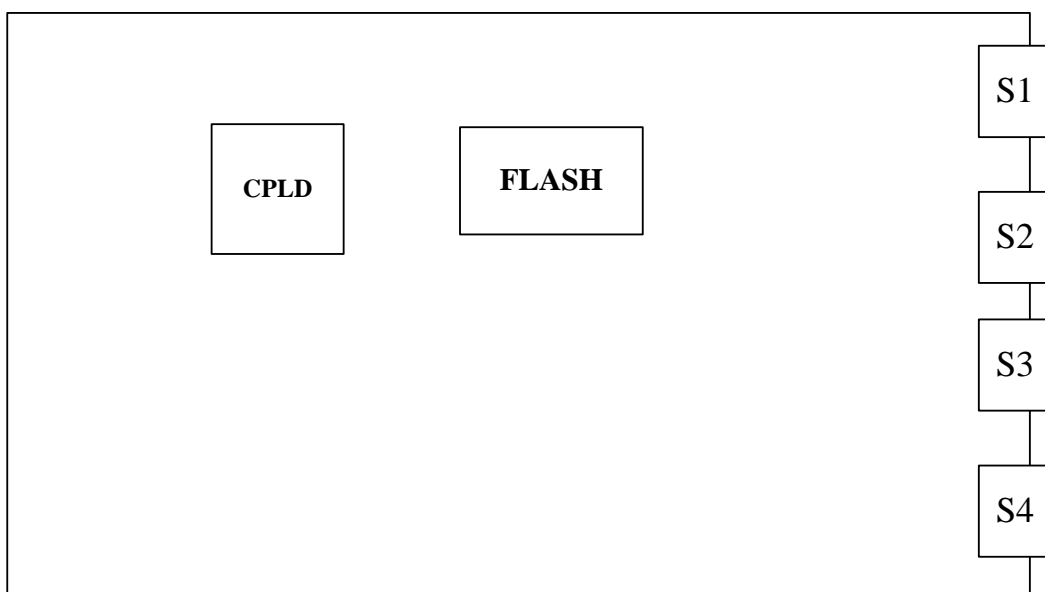
2.2.3 Location Overview

Figure 3 highlights the position of the important components. Depending on the board type it may be that your board does not include all components shown in the location diagram.

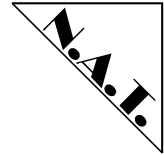
Figure 3: Location diagram of the **NPMC-860-4S0** (schematic)



Top View



Bottom View



2.3 Automatic Power Up

In the following situations the **NPMC-860-4S0** will automatically be reset and proceed with a normal power up.

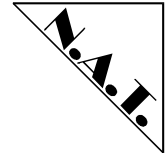
Voltage sensor

The voltage sensor generates a reset

- when +5V voltage level drops below 4,6V
- when +5V voltage level rises above 5,4V
- or when the carrier board signals a PCI Reset

Watchdog timer

Per factory default the watchdog timer of the PowerQUICC is disabled. If the watchdog timer is enabled, it generates a non-maskable interrupt (NMI) followed by a reset when it is not retriggered by software (see the PowerQUICC users manual).



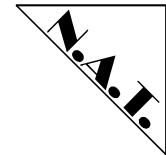
3 Hardware Details

3.1 Memory Map

All addresses are set up by programming the corresponding Chip-Select Decoder of the PowerQUICC.

Table 2: NPMC-860-4S0 Memory Map

Device	CS Line	Function	Notes
Flash-PROM	CS0	CS for FLASH	2/4 MByte Flash-Prom (8 Bit wide)
DRAM	CS1	CS for DRAM	4/16 MByte EDO DRAM (32 Bit wide)
	CS2	not used	
PCI	CS3	CS for PMC → PCI bus access	there are two PCI images available selected by the IMS-Signal. This Signal is generated by the Port D Bit 15
QSPAN	CS4	Qbus access to the QSPAN II Registers	
TSI	CS5	CS for the TSI	
	CS6	not used	
I/O	CS7	CPLD Registers, SCbus ID	a number of control/status registers is implemented in a CPLD



3.2 PowerQUICC Port Pins Usage

Table 3: PowerQUICC Port Pin Usage (Port A)

Signal Function	PowerQUICC Port A Pin	Description
DGNT1	PA15	GNT signal for S/T port 1
DREQ4	PA14	REQ signal for S/T port 4
MC TxD	PA13	Message Channel Transmit
MC RxD	PA12	Message Channel Receive
IDL RxD	PA11	IDL Channel Receive
IDL TxD	PA10	IDL Channel Transmit
TSI LSII	PA9	Time Slot Assigner Bus data bit 1, output of MPC860, input to ML53812 H.110 controller (Time Slot Interchange (TSI))
TSI LSO1	PA8	Time Slot Assigner Bus data bit 1, input to MPC860, output of ML53812 H.110 controller (Time Slot Interchange (TSI))
IDL DCL	PA7	IDL bus clock
MC CLK	PA6	Message Channel clock
IDL DCL	PA5	IDL bus clock
DREQ3	PA4	REQ signal for S/T port 3
DREQ2	PA3	REQ signal for S/T port 2
IDL DCL	PA2	IDL bus clock
DREQ1	PA1	REQ signal for S/T port 1
IDL DCL	PA0	IDL bus clock

Table 4: PowerQUICC Port Pin Usage (Port B)

Signal Function	PowerQUICC Port B Pin	Description
not used	PB31	not used
SPI CLK	PB30	SPI bus clock
SPI RX	PB29	SPI bus Receive
SPI TX	PB28	SPI bus Transmit
SDA_PQ	PB27	I ² C data
SCL_PQ	PB26	I ² C clock
SMC1 TxD	PB25	SMC1 Channel Transmit
SMC1 RxD	PB24	SMC1 Channel Receive
/SDACK1	PB23	DMA Ack to QSpan II
not used	PB22	not used
PZMP4*	PB21	Point-to-Multi-Point channel 4
PZMP3*	PB20	Point-to-Multi-Point channel 3
PZMP2*	PB19	Point-to-Multi-Point channel 2
PZMP1*	PB18	Point-to-Multi-Point channel 1
NT4*	PB17	TE/NT selection channel 4
NT3*	PB16	TE/NT selection channel 3
NT2*	PB15	TE/NT selection channel 2
NT1*	PB14	TE/NT selection channel 1

Signals with asterisk (*) are described in detail below.

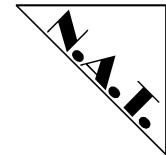


Table 5: PowerQUICC Port Pin Usage (Port C)

Signal Function	PowerQUICC Port C Pin	Description
/DREQ1	PC15	DMA REQ from QSpan II
DGNT4	PC14	GNT signal for S/T port 4
DGNT3	PC13	GNT signal for S/T port 3
DGNT2	PC12	GNT signal for S/T port 2
/IRQST4	PC11	Interrupt S/T port 4
/IRQST3	PC10	Interrupt S/T port 3
/IRQST2	PC9	Interrupt S/T port 2
/IRQST1	PC8	Interrupt S/T port 1
IDL FS	PC7	IDL bus frame sync
IDL FS	PC6	IDL bus frame sync
IDL FS	PC5	IDL bus frame sync
IDL FS	PC4	IDL bus frame sync

Table 6: PowerQUICC Port Pin Usage (Port D)

Signal Function	PowerQUICC Port D Pin	Description
IMSEL	PD15	Image Select for QSpan II
LED4*	PD14	Front Panel LED
LED3*	PD13	Front Panel LED
LED2*	PD12	Front Panel LED
LED1*	PD11	Front Panel LED
not used	PD10	
not used	PD9	
not used	PD8	
not used	PD7	
SEL ST4*	PD6	enable S/T port 4
SEL ST3*	PD5	enable S/T port 3
SEL ST2*	PD4	enable S/T port 2
SEL ST1*	PD3	enable S/T port 1

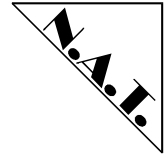
All port signals are tristate after Power-Up, until programmed differently. Output signals marked with an asterisk (*) are described below in their (active) low state:

PZMP1 – 4 selection of point-to-point or point-to-multi-point connection,
low = point-to-point, high = point-to-multi-point

NT1 – 4 selection of TE/NT interface, low = TE (default), high = NT

LED1 – 4 lit when set low

SEL ST1 – 4 enable S/T ports, low = enabled



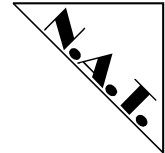
3.3 Interrupt Structure

The **NPMC-860-4S0** has the following interrupt structure:

Table 7: NPMC-860-4S0 Interrupt Structure

Interrupt source	PowerQUICC Interrupt level
NC	IRQ-Level 0 (highest level)
for future use	IRQ-Level 1
QSPAN II	IRQ-Level 2
TSI	IRQ-Level 3
NC	IRQ-Level 4
NC	IRQ-Level 5
NC	IRQ-Level 6
for future use	IRQ-Level 7 (lower level)

The interrupt pins of the 4 S0 interface chips are routed to the port pins PC8 - PC11 of the PowerQUICC, which are capable of generating interrupts. They are not routed to dedicated IRQ-pins.



3.4 Control / Status Registers

MPC860 CS7 (CSIO) selects the Control / Status Registers. The address range decoded by hardware is 4 bytes. Larger address ranges mirror every 4 bytes.

Pure Status Registers are read-only, Status / Control Registers are read/write.

3.4.1 Status Register 1

Status Register 1 is accessed with address offset 0x0 to the CSIO base address programmed for CS7. By means of this register the SCbus slot address is readable.

Table 8: Status Register 1

Bit Number	Read/Write	Status Information
Bit 7	R	not used, reads as 0
Bit 6	R	not used, reads as 0
Bit 5	R	not used, reads as 0
Bit 4	R	SCbus slot address bit SL_4
Bit 3	R	SCbus slot address bit SL_3
Bit 2	R	SCbus slot address bit SL_2
Bit 1	R	SCbus slot address bit SL_1
Bit 0	R	SCbus slot address bit SL_0

3.4.2 Control/Status Register 2

Control/Status Register 2 is accessed with address offset 0x4 to the CSIO base address programmed for CS7. By means of this register the status of the Timeout bits is readable.

The Timeout bits are generated in a CPLD and mirror the activity of a TE port. If a TE port is active, i.e. generates a SYNC signal to the logic, the corresponding Timeout bit will read 0. If there is no (more) activity on this port, hence it is no longer suitable to be source of local synchronisation, the corresponding Timeout bit will read 1.

These bits are implemented for applications where there is no TSI device assembled. Additional information on this is available on request. As by default the TSI device is assembled, the Timeout bits are not used in a standard application.

Also, for NT mode the FIX pins of the MC145574 S/T framers are settable/readable. By means of these bits fixed / adaptive timing can be selected. Refer to the MC145574 manual for further details.

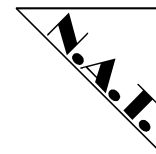


Table 9: Control/Status Register 2

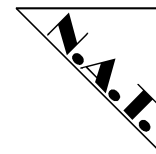
Bit Number	Read/Write	Status Information
Bit 7	R	TIMEOUT bit of the MC145574 S/T framer port 4
Bit 6	R	TIMEOUT bit of the MC145574 S/T framer port 3
Bit 5	R	TIMEOUT bit of the MC145574 S/T framer port 2
Bit 4	R	TIMEOUT bit of the MC145574 S/T framer port 1
Bit 3	R/W	FIX bit of the MC145574 S/T framer port 4
Bit 2	R/W	FIX bit of the MC145574 S/T framer port 3
Bit 1	R/W	FIX bit of the MC145574 S/T framer port 2
Bit 0	R/W	FIX bit of the MC145574 S/T framer port 1

3.4.3 Status Register 3

Status Register 3 is accessed with address offset 0x8 to the CSIO base address programmed for CS7. By means of this register the status of the TSEN pins of the framers are readable. Refer to the MC145574 manual for further details.

Table 10: Status Register 3

Bit Number	Read/Write	Status Information
Bit 7	R	not used, reads as 0
Bit 6	R	not used, reads as 0
Bit 5	R	not used, reads as 0
Bit 4	R	not used, reads as 0
Bit 3	R	TSEN pin framer 4
Bit 2	R	TSEN pin framer 3
Bit 1	R	TSEN pin framer 2
Bit 0	R	TSEN pin framer 1



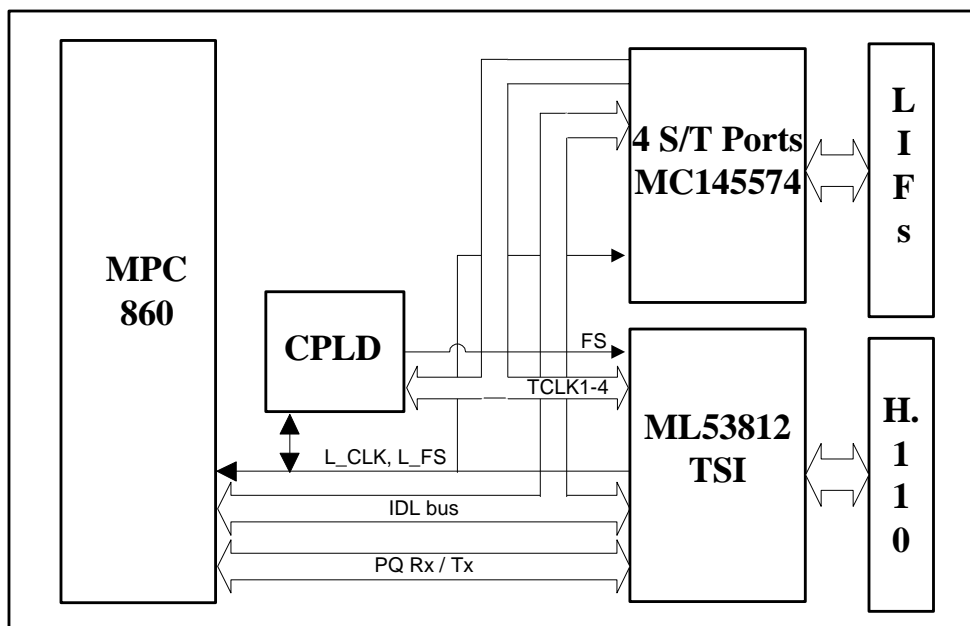
3.5 IDL Bus Operation

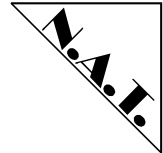
The four S/T ISDN framers, the MPC860 CPU TDM port, and the ML52812 H.110 TSI device are interconnected by an IDL bus. This IDL bus is mastered either by one of the framers, or by the TSI device. The IDL bus master provides a Sync signal to a LREF input of the TSI device, which generates local sync and clock for the IDL bus from it. Any framer and the TSI device (if SCbus/H.110 bus slave) can be sync source for the IDL bus. This is either decided by software, or by hardware implemented in a CPLD, which chooses an active TE port to be master, and switches to another active one, if the one it is locked to goes inactive. If there is no active port at all, a free running mode may be selected. Which port is sourcing a valid sync can also be read from Control/Status Register 2 described above. The TIMEOUT bits for each port read 1, if there is no carrier detected by the S/T chip, and reads 0, if the S/T chip locks to the line.

3.6 Time Division Multiplex Bus Structure

The TDM bus structure connects the IDL bus of the framers to the local TDM bus between CPU and TSI device, and to the backplane SCbus/H.110 bus. Timeslot assignment is done within the framers and the CPU, switching of timeslots between the different devices and the backplane is done by the TSI device. The TDM interconnect structure is shown below:

Figure 4: TDM Bus Organisation and Synchronisation

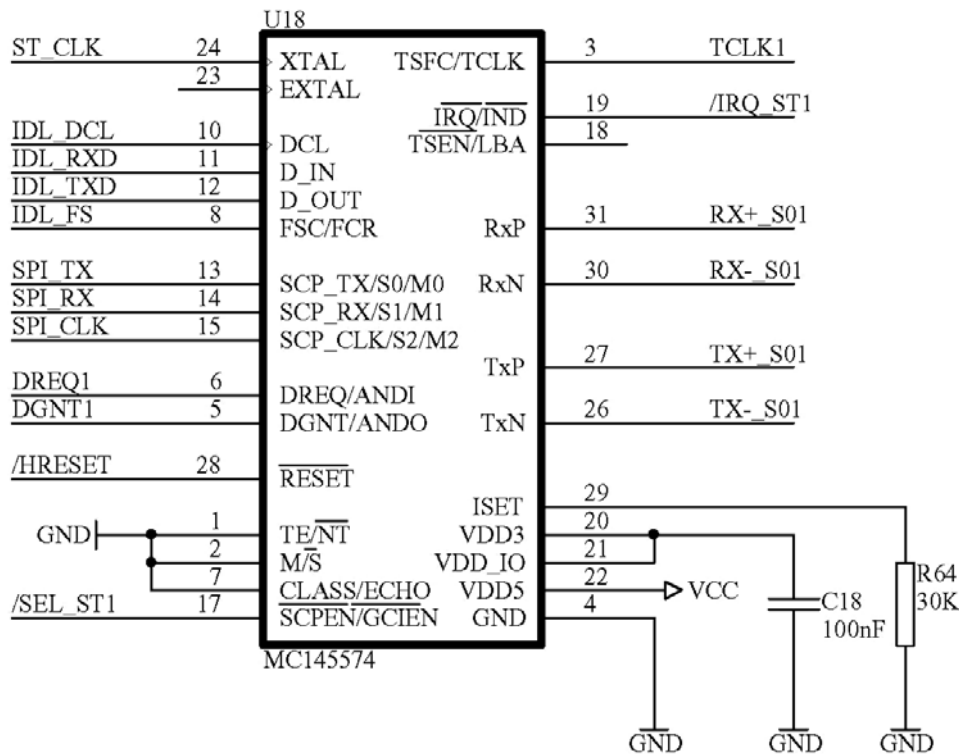




3.7 S/T Port Setup

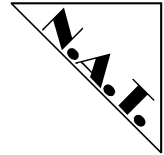
The following figure shows the connections of a S/T port device. All 4 port devices are connected alike.

Figure 5: S/T Port Setup



The IDL bus (described above) connects the framers to the TSI device. The S/T port devices are programmed by the SPI port of the MPC860. DREQ, DGNT, SCP-/GCIEN are connected to CPU port pins and thus programmable for any application's needs. The TCLK signal may fulfill different tasks: clock output, sync output in TE mode, or FIX input in NT mode. Hence, the CPLD pins the TCLKx signals are connected to may be programmed as input or output. This depends on the setting of the NTx inputs connected to CPU port pins. If a channel is set to be NT (and the corresponding CPU port pin NTx is set accordingly), the CPLD TCLKx pin will be an output and drive the logic state programmed in the FIXx bits of the Control/Status Register 2 described above.

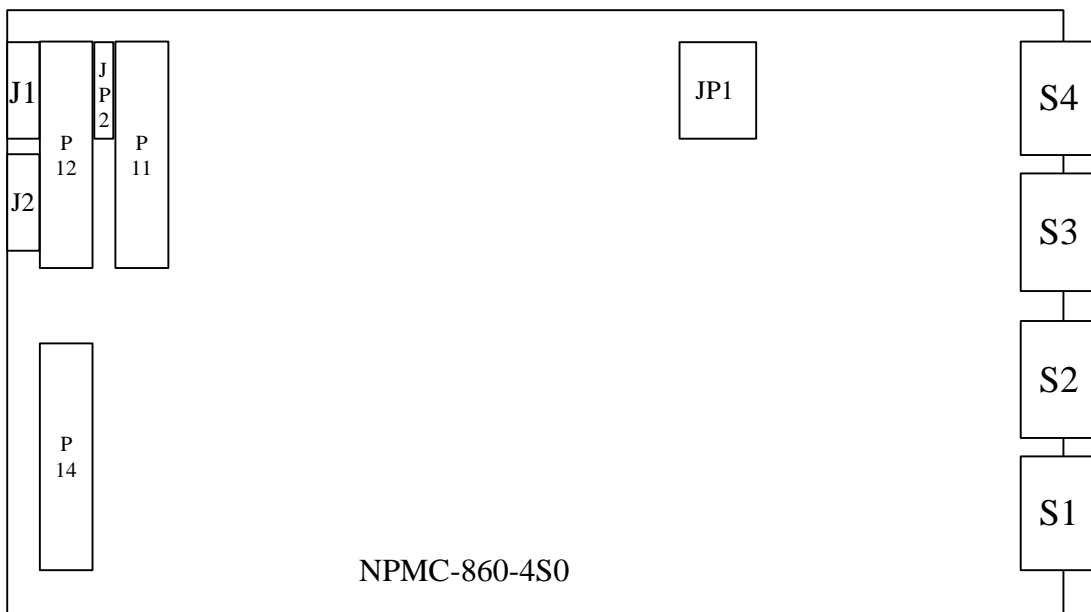
Please refer to the MC145574 User's Manual for additional information. Sample driver code is available from N.A.T..



4 Connectors

4.1 Connector Overview

Figure 6: Connectors of the NPMC-860-4S0

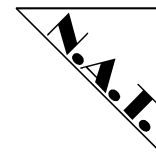


4.2 Switch Settings

Jumper J1 is used for a Background Debug Mode Tool. This is a Power-Up option. If a BDM tool is to be used, J1 needs to be installed **before** powering up the module.

Default: J1 not installed

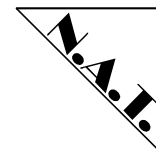
Jumper J2 is used for factory test and its setting should not be altered by the user. Therefore, J2 is not assembled by default.



4.3 PMC Connector P11

Table 11: PMC Connector P11

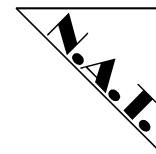
Ext. Signal	Pin No.	PCI-Signal	PCI-Signal	Pin No.	Ext. Signal
N.C.	1	TCK	-12V	2	N.C.
GND	3	GND	/INT A	4	/IRQ-QSPAN
N.C.	5	/INT B	/INT C	6	N.C.
N.C.	7	bus mode 1	+5V	8	+5V
N.C.	9	/INT D	PCI_RSV1	10	N.C.
GND	11	GND	PCI_RSV2	12	N.C.
CLK	13	CLK	GND	14	N.C.
GND	15	GND	/GNT	16	/GNT
/REQ	17	/REQ	+5V	18	+5V
N.C.	19	V (I/O)	AD31	20	PCI_AD31
PCI_AD28	21	AD28	AD27	22	PCI_AD22
PCI_AD25	23	AD25	GND	24	GND
GND	25	GND	CBE3	26	/CBE3
PCI_AD22	27	AD22	AD21	28	PCI_AD21
PCI_AD19	29	AD19	+5V	30	+5V
N.C.	31	V (I/O)	AD17	32	PCI_AD17
/FRAME	33	/FRAME	GND	34	GND
GND	35	GND	/IRDY	36	/IRDY
/DEVSEL	37	/DEVSEL	+5V	38	+5V
GND	39	GND	/LOCK	40	N.C.
N.C.	41	/SDONE	/SB0	42	N.C.
PAR	43	PAR	GND	44	GND
N.C.	45	V (I/O)	AD15	46	PCI_AD15
PCI_AD12	47	AD12	AD11	48	PCI_AD11
PCI_AD09	49	AD09	+5V	50	+5V
GND	51	GND	/CBE0	52	/CBE0
PCI_AD06	53	AD06	AD05	54	PCI_AD05
PCI_AD04	55	AD04	GND	56	GND
N.C.	57	V (I/O)	AD03	58	PCI_AD03
PCI_AD02	59	AD02	AD01	60	PCI_AD01
PCI_AD00	61	AD00	+5V	62	+5V
GND	63	GND	/REQ64	64	N.C.



4.4 PMC Connector P12

Table 12: PMC Connector P12

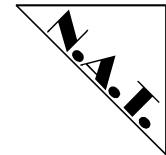
Ext. Signal	Pin No.	PCI-Signal	PCI-Signal	Pin No.	Ext. Signal
N.C.	1	+12V	/TRST	2	N.C.
N.C.	3	TMS	TDO	4	N.C.
N.C.	5	TDI	GND	6	GND
GND	7	GND	PCI_RS3V3	8	N.C.
N.C.	9	PCI_RS3V3	PCI_RS3V3	10	N.C.
N.C.	11	BUS-MODE 2	+3.3V	12	+3.3V
/RST	13	/RTS	BUS-MODE 3	14	N.C.
+3.3V	15	+3.3V	BUS-MODE 4	16	N.C.
N.C.	17	PCI_RS3V3	GND	18	GND
PCI_AD30	19	AD30	AD29	20	PCI_AD29
GND	21	GND	AD26	22	PCI_AD26
PCI_AD24	23	AD24	+3.3V	24	+3.3V
/IDSEL	25	IDSEL	AD23	26	PCI_AD23
+3.3V	27	+3.3V	AD20	28	PCI_AD20
PCI_AD18	29	AD18	GND	30	GND
PCI_AD16	31	AD16	/CBE2	32	/CBE2
GND	33	GND	PCI_RESVD	34	N.C.
/TRDY	35	/TRDY	+3.3V	36	+3.3V
GND	37	GND	/STOP	38	/STOP
/PERR	39	/PERR	GND	40	GND
+3.3V	41	+3.3V	/SERR	42	/SERR
/CBE1	43	/CBE1	GND	44	GND
PCI_AD14	45	AD14	AD13	46	PCI_AD13
GND	47	GND	AD10	48	PCI_AD10
PCI_AD08	49	AD08	+3.3V	50	+3.3V
PCI_AD07	51	AD07	PCI_RESV	52	N.C.
+3.3V	53	+3.3V	PCI_RESV	54	N.C.
N.C.	55	PCI_RESV	GND	56	GND
N.C.	57	PCI_RESV	PCI_RESV	58	N.C.
GND	59	GND	PCI_RESV	60	N.C.
N.C.	61	ACK64	+3.3V	62	+3.3V
GND	63	GND	PCI_RESV	64	N.C.



4.5 Pin Assignment of the PMC Connector -- P14 (PMC I/O)

Table 13: Pin Assignment of the PMC Connector -- P14

ext. Signal	Pin No.	PCI-Signal	PCI-Signal	Pin No.	ext. Signal
MC	1	I/O	I/O	2	CT_D15
CT_D14	3	I/O	I/O	4	CT_D13
CT_D12	5	I/O	I/O	6	GND
CT_D11	7	I/O	I/O	8	CT_D10
CT_D09	9	I/O	I/O	10	CT_D8
CT_D07	11	I/O	I/O	12	GND
CT_D06	13	I/O	I/O	14	CT_D5
CT_D04	15	I/O	I/O	16	CT_D3
CT_D02	17	I/O	I/O	18	CT_D1
GND	19	I/O	I/O	20	CT_D0
CLKFAIL	21	I/O	I/O	22	/FSYNC
SREF_8K	23	I/O	I/O	24	SCLK
GND	25	I/O	I/O	26	/SCLKx2
SL_4	27	I/O	I/O	28	/C16+
SL_2	29	I/O	I/O	30	SL_3
SL_0	31	I/O	I/O	32	SL_1
nc	33	I/O	I/O	34	nc
nc	35	I/O	I/O	36	nc
/C16-	37	I/O	I/O	38	CT_FRAME_B
CT_FRAME_A	39	I/O	I/O	40	CT_NETREF2
CT_NETREF1	41	I/O	I/O	42	/C4
C2	43	I/O	I/O	44	GND
CT_C8_B	45	I/O	I/O	46	CT_C8_A
CT_D16	47	I/O	I/O	48	CT_D17
CT_D18	49	I/O	I/O	50	CT_D19
GND	51	I/O	I/O	52	CT_D20
CT_D21	53	I/O	I/O	54	CT_D22
CT_D23	55	I/O	I/O	56	CT_D24
GND	57	I/O	I/O	58	CT_D25
CT_D26	59	I/O	I/O	60	CT_D27
CT_D28	61	I/O	I/O	62	CT_D29
CT_D30	63	I/O	I/O	64	CT_D31



4.5.1 Description P14 Signals

Table 14: Description P14 Signals

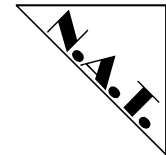
Signal	Description VITA Spec.	Description General
MC	identical	SCBus message channel
CT_D0 - 15	SD_0 - 15	SCBus/H.110 serial data stream 0 - 15
CLKFAIL	identical	SCBus System Clock Fail signal
SREF_8K	SREF8k	SCBus 8 kHz reference signal
SL_0 - 4	identical	SCBus ID
SCLKx2N	SCLKx2	SCBus System clock x 2.
SCLK	SCLK	SCBus System clock.
FSYNCN	FSYNC	SCBus 8 kHz frame signal
CT_D16 - 31	not defined	H.110 serial data stream 16 - 31
C2	not defined	H.110 2 MHz clock
/C4	not defined	H.110 4 MHz clock
/C16+	not defined	H.110 16 MHz differential clock
/C16-	not defined	H.110 16 MHz differential clock
CT_FRAME_A	not defined	H.110 8 kHz frame signal
CT_FRAME_B	not defined	H.110 8 kHz frame signal
CT_C8_A	not defined	H.110 8 MHz clock
CT_C8_B	not defined	H.110 8 MHz clock
CT_NETREF1	not defined	H.110 8 kHz reference signal
CT_NETREF2	not defined	H.110 8 kHz reference signal

For more details please refer to the VITA *Extensions to ANSI/VITA 6 - 1994 SCSA*.

4.5.2 SCbus IDs

In every SCSA system each SCSA device needs to have a unique ID.

The NPMC-860-4S0 supports reading the setting of SC IDs on the VMEbus / cPCI bus backplane. This is done by reading Status Register 1 as described above.



4.6 The Front Panel Connectors (S1 - S4)

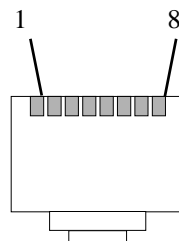
The front panel connectors are RJ45 connector (8 pins). The 4 S0 line interfaces are available on the pins of the front panel connectors. Table 5 shows the pin assignment.

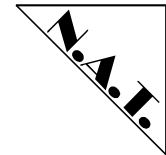
Table 15: General Pin Assignment of the Front-panel Connectors S1 - 4

RJ45 Pin	3	6	4	5
Signal NT	TX+	TX-	RX+	RX-
Signal TE	RX+	RX-	TX+	TX-

Rx/Tx can be swapped for TE/NT application by software. This feature, apart from some others, needs reprogramming of the I/O port pins of the PowerQUICC. Refer to the software documentation for further details.

RJ 45 male connector (front view)





4.7 Connector JP1: Motorola Background Debug Mode (BDM)

The RS232 serial I/O port is available via a 20 pin SMD micro connector together with the JTAG / BDM Port (see JP1 in the location overview).

The RS232 port is realised with the PowerQUICC serial communication controller SMC1.

Jumper J1 enables the Background Debug Mode (BDM), when installed. Default: J1 removed.

Table 16: JP1 BDM and IEEE 1149.1 Connector Pinout Options

JTAG					
BDM Port					
PIN					
	VFLS0	1		2	/SRESET
GND	GND	3		4	DSCK
GND	GND	5		6	VFLS1
	/HRESET	7		8	DSDI
+5V	+5V	9		10	DSDO
		11		12	TMS
	FRZ	13		14	+3.3V
		15		16	GND
RXD_SMC1	RXD_SMC1	17		18	GND
TXD_SMC1	TXD_SMC1	19		20	GND

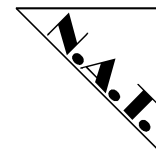
An adapter board with cable plugging into the 20 pin SMD micro connector is available from N.A.T., that connects the JP1 connector to a standard 2-row, 10-pin, 100mil header used for BDM tool boxes, and routes the additional RS232 debug port signals to a standard 9-pin SubD female connector.

4.8 Connector JP2: Lattice Programming Port

Connector JP2 connects the JTAG- or programming-port of the Lattice CPLD device.

Table 17: Lattice Programming Port

Pin No.	Signal	Signal	Pin No.
1	TCK	nc	2
3	TMS	GND	4
5	TDI	+3.3V	6
7	TDO	GND	8
9	/TRST	/ENABLE	10



5 Software Application Notes

5.1 Host Setup of the QSpan II PCI Bridge

In order to configure the **NPMC-860-4S0** to work on the PCI-bus, the following steps must be taken:

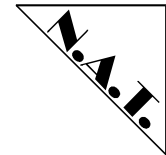
1. Look up the address of the PCI-bus controller of the **NPMC-860-4S0** in the *Configuration Space* of the PCI-bus of the carrier board (please refer to the manual for the carrier board).
The PCI-bus controller of the **NPMC-860-4S0** occupies 256 Bytes in the *Configuration Space* and you should see the following address map (first 64 bytes according to PCI specification 2.1):

Table 18: NPMC-860-4S0 memory map in the configuration space

Offset	QSpan register	Description of register
0x0000	PCI_ID	ID, start address configuration space
0x0004	PCI_CS	control and status
0x0008	PCI_CLASS	class
0x000c	PCI_MISC0	miscellaneous 0
0x0010	PCI_BSM	base address for memory
...
0x003c	PCI_MISC1	miscellaneous 1

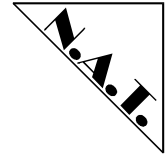
For more details regarding the QSpan II registers of the **NPMC-860-4S0**, please refer to the QSpan II manual's register map (table A.1, Appp. A-2).

2. Now write - to the offset address 0x0010 (QSpan II register PCI_BSM, 32 bit) - the start address of the **NPMC-860-4S0** where it should appear in the *memory space* of the carrier board's PCI-bus. Please note, that all PCI register accesses have to be done in little endian format.
The register image of the QSpan II should now be visible in the PCI memory space.

**Table 19:** NPMC-860-4S0 memory map in the PCI memory space

Offset	QSpan II register	Description of register
0x0000	PCI_ID	ID, start address QSpan register
0x0004	PCI_CS	control and status
0x0008	PCI_CLASS	Class
0x000c	PCI_MISC0	miscellaneous 0
0x0010	PCI_BSM	base address for memory
0x0014	-	QSpan unimplemented
...
0x003c	PCI_MISC1	miscellaneous 1
...
0x800	MISC_CTL	miscellaneous control
0x804	EEPROM_CS	EEPROM control
...
0x0ffc	-	QSpan reserved

3. Initialize the register PBTIO_CTL for target image 0 and set the necessary parameters:
The longword read/write access must be enabled by writing the PBTIO_CTL at offset 0x0100 (image enable, block size BS[3:0] = 0110 = 4 MB, or BS[3:0] = 1000 = 16 MB, Q-bus destination port size DSIZE[1:0] = 00 = 32 bit).
4. Set address translation decoding on register PBTIO_ADD at offset 0x0104 (host system dependent):
Write the start address where the memory of the NPMC-860-4S0 module should appear in the *Memory Space* of the PCI bus.
5. Make certain that there are no address conflicts in your systems (set/check the amount of the memory occupied by the **NPMC-860-4S0** in the PCI memory space).



5.2 Q-Bus Configuration

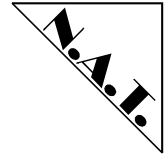
Through the MISC_CTL register parameters for configuring the local bus (Q-Bus) are set. The settings to be performed are system dependant. But, the following aspect has to be taken into account in any case:

Setting of bit 0 (SW-RST) will cause a RESET on the Q-Bus, if the Q-BUS HRESET signal is connected to the RESETO pin of the QSPAN (like for this module). The RESETO signal follows the programming of the SW-RST bit directly, i.e. without any delay in time. Therefore, if the MPC860 is to be reset by this means, the minimum time period necessary to perform an orderly hardware reset of the MPC860 has to be strictly obeyed. Otherwise the MPC860 may enter an undefined state. A time period of 100ms is recommended between the setting and resetting of this bit. In time-critical applications this period may be reduced. Any value longer than 1ms should be sufficient. 100ms is a period of time which is suitable and safe for resetting the Q-Bus in all cases and for all CPU operating frequencies.

5.3 EEPROM Configuration

By means of register EEPROM_CS the Configuration-EEPROM may be read and reprogrammed, which the QSPAN II uses for Power-Up – initialialisation. Please be aware of the fact that programming the EEPROM with unsuitable values may cause the PCI-Bus to hang completely.

NOTE: For more information, please refer to the QSpan II manual. Please make certain that you use the correct endian format when writing into the QSpan II registers.



Annex A PowerQUICC CPU

Introduction

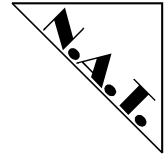
The MPC860 PowerPC™ Quad Integrated Communications Controller (PowerQUICC) is a versatile one-chip integrated microprocessor and peripheral controller combination that can be used in a variety of applications. It particularly excels in both communications and networking systems.

The MPC860 is a PowerPC-based derivative of Motorola's MC68360 (Quad Integrated Communications Controller (QUICC™)). The CPU on the MPC860 is a 32-bit PowerPC implementation that incorporates memory management units (MMUs) and instruction and data caches. The communications processor module (CPM) of the MC68360 QUICC has been enhanced with the addition of the interprocessor-integrated-controller (I²C) channel. Moderate to high digital signal processing (DSP) functionality has been added to the CPM. The memory controller has been enhanced, enabling the MPC860 to support any type of memory, including high performance memories and newer dynamic random access memories (DRAMs).

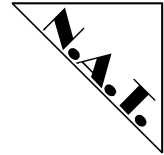
Features

The following is a list of the MPC860's important features:

- PowerPC single issue integer core
- High performance (52 K Dhrystone 2.1 MIPS @ 50MHZ, 3,3V, 1.3Watts total power)
- MPC860 PowerPC system interface, including a periodic interrupt timer, a bus monitor, and real-time clocks
- 32-bit address and data busses
- Flexible memory management
- 4-kbyte physical address, two-way, set-associative data cache
- 4-kbyte physical address, two-way, set-associative instruction cache
- Eight-bank memory controller
- System interface unit
- Communications processor module
 - Embedded 32-bit RISC controller architecture for flexible I/O
 - Interfaces to PowerPC core through on-chip dual-port RAM and virtual DMA channel controller
 - Continuous mode transmission and reception on all serial channels
 - Serial DMA channels for reception and transmission on all serial channels
 - Parallel I/O-registers with open-drain and interrupt capability



- Protocols supported by ROM or downloadable microcode and include, but are not limited to, the digital portions of:
 - Ethernet / IEEE 802.3 CS/DMA
 - HDLC2 / SDLC and HDLC bus
 - AppleTalk
 - Signalling system #7 (RAM microcode only)
 - Universal asynchronous receiver transmitter (UART)
 - Synchronous UART
 - Binary synchronous (BiSync) communications
 - totally transparent
 - totally transparent with CRC
 - Profibus (RAM microcode only)
 - Asynchronous HDLC
 - DDCMP
 - V.14 (RAM microcode only)
 - X.21 (RAM microcode only)
 - V.32bis datapump filters
 - IrDA serial infrared
 - Basic rate ISDN (BRI) in conjunction with SMC channels
 - Primary rate ISDN (MH-Chip version only)
- Four hardware serial communications controller channels supporting the above protocols
- Two hardware serial management channels
 - Provide management for BRI devices as general circuit interface controller in time division multiplexed channels
 - Transparent and low speed UART operation
- I²C (microwire compatible) interface
 - Supports master and slave modes
- Time slot assigner
 - Supports one or two TDMA channels
 - Bit or byte resolution
 - Independent transmit and receive routing, frame synchronisation, clocking able to be dynamically modified
 - Can be configured by software for internal interconnection of CPM serial channels
 - Typically implements T1, CEPT, PCM highway, ISDN basic rate, ISDN primary rate and user-defined TDMA serial interfaces
- Parallel interface port supports Centronics interfaces and chip-to-chip interconnection
- Four independent baud rate generators and four input clock pins for supplying clocks to SMC and SCC serial channels
- Four independent 16-bit timers which can be used as two 32-bit timers



Annex B QSpan IITM Bus Bridge

Introduction

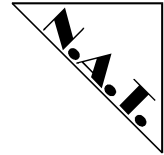
The QSpan IITM chip is a member of Tundra Semiconductor Corporation's family of PCI bus-bridging devices enabling board designers to bring PCI-based embedded products to market faster and for less cost.

The QSpan IITM is designed to gluelessly bridge the QUICCTM (MC68360), the PowerQUICCTM as well as the MPC801 embedded controllers to PCI.

Features

The QSpan IITM has the following features:

- A direct connect interface to the PCI bus for Motorola's QUICC (MC68360), PowerQUICC(MPC860), M68040, the PMC821 and the MPC861 embedded controllers;
- 32-bit PCI interface compliant with PCI Revision 2.1;
- Decoupled transfer technology: three 16-entry deep FIFOs buffer multiple transaction in both directions, allowing zero wait state bursting on the PCI and Motorola buses;
- IDMA peripheral support for QUICC and PowerQUICC;
- Flexible address space mapping and translation between the PCI and Motorola buses;
- Programmable endian byte ordering;
- Two user-programmable slave images available for PCI access to the Motorola buses;
- QSpan IITM control and status registers accessible from both PCI and Motorola buses;
- PCI bus and Motorola buses can be operated at different clock frequencies;



Annex C RAM/ROM

DRAM

The **NPMC-860-4S0** provides an on-board DRAM (EDO-DRAM). This memory is accessible from the PowerQUICC or the QSPAN II PCI-bridge chip. The memory controller of the PowerQUICC is responsible for controlling the DRAM. This flexible memory controller allows the implementation of memory systems with very specific timing requirements.

The user is allowed to define different timing patterns for the control signals that govern a memory device. These patterns define how the external control signals behave in a read-access request, write-access request, burst read-access request, or burst write-access request. The user defines how the external control signals toggle when the periodic timers reach the maximum programmed value for refresh operation.

The memory capacity is 4 MByte (optionally 16 MByte), the memory is 32 bit wide. The access time of the EDO DRAM is 60 nsec for new accesses, the access time within a row is 30 nsec (bursting)

For different operating frequency of the MPC860 the user needs to define different timing patterns.

The User Programmable Machine A (UPM A) controls the PowerQUICC and the PCI accesses to the DRAM memory.

In the PowerQUICC Reset-state accesses to the DRAM will be inhibited.

Parity generation and check will not be supported by the module

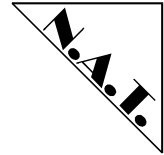
Boot Flash

The flash memory area is located on the PowerQUICC bus so that the reset vector table in the boot flash is visible to the CPU after power on reset. The boot flash memory has a size of 2 MByte (optionally 4 MByte) and can be directly accessed by the CPU. The flash memory area is 8-bit wide organized.

The flash memory is a 5V only device. For programming the Flash no extra programming voltage is necessary.

Programming the flash memory is possible in two ways:

- Programming the entire flash memory from the PCI-bus. The module must be in the RESET-State.
- Programming the flash memory in the run state of the PowerQUICC.



Annex D Documentation reference

PCI Interface chip

Company: TUNDRA
Title: QSPAN II (CA91CC862)
PCI to Motorola Processor Bridge Manual

MPC860 PowerQUICC

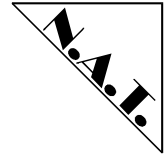
Company: Motorola Inc.
Title: MPC860 PowerQUICC
User's Manual

Timeslot Switching Interface chip

Company: Oki
Title: ML53812-2 H.100/H.110 CT Bus System Interface and Time-Slot Interchange
User's Manual

S0 Line Interface chip

Company: Motorola
Title: MC145574 ISDN S/T Interface Transceiver
User's Manual



Annex E Document's History

Version	Date	Description	Name
0.9	10. Sept. 98	initial revision	mz
	28.07.1999	Layout improvements	as
	30.08.1999	correction of figures 3 and 4 added table 6 (debug port)	as
1.0	21.06.2001	chapter 3.1 (QSPAN) reworked	ga
1.1	04.08.2003	adapted to HW revision 1.1	ga
1.2	05.09.2003	adapted to HW revision 2.0	ga
1.3	22.08.2005	Figure 4 corrected	ga