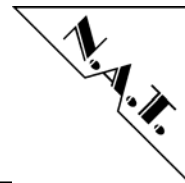


# **NPMC-DSP**

**PMC Module for Telecom  
Applications**

**Technical Reference Manual V1.1  
Hardware Revision V1.3**



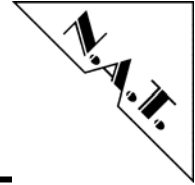
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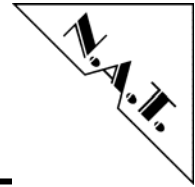
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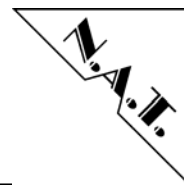
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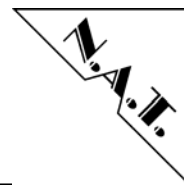
# Table of Contents

<b>TABLE OF CONTENTS</b> .....	<b>4</b>
<b>LIST OF FIGURES</b> .....	<b>6</b>
<b>LIST OF TABLES</b> .....	<b>6</b>
<b>CONVENTIONS</b> .....	<b>7</b>
<b>1 INTRODUCTION</b> .....	<b>8</b>
1.1 BOARD FEATURES .....	10
1.2 BOARD SPECIFICATION .....	11
<b>2 INSTALLATION</b> .....	<b>12</b>
2.1 SAFETY NOTE .....	12
2.2 INSTALLATION PREREQUISITES AND REQUIREMENTS .....	13
2.2.1 <i>Requirements</i> .....	13
2.2.2 <i>Power supply</i> .....	13
2.2.3 <i>Automatic Power Up</i> .....	13
2.3 STATEMENT ON ENVIRONMENTAL PROTECTION .....	14
2.3.1 <i>Compliance to RoHS Directive</i> .....	14
2.3.2 <i>Compliance to WEEE Directive</i> .....	14
2.4 LOCATION OVERVIEW .....	15
<b>3 FUNCTIONAL BLOCKS</b> .....	<b>16</b>
3.1 DSPs .....	16
3.2 PCI INTERFACE.....	17
3.3 MEMORY .....	17
3.3.1 <i>SDRAM</i> .....	17
3.3.2 <i>FLASH</i> .....	17
3.3.3 <i>EEPROM</i> .....	17
3.3.4 <i>I<sup>2</sup>C Device</i> .....	17
3.4 H.110 BUS CONTROLLER.....	18
3.4.1 <i>Block Diagramm of the TDM Structure</i> .....	18
3.4.2 <i>Description of the TDM Structure</i> .....	18
3.4.3 <i>SCbus Compatibility</i> .....	19
<b>4 HARDWARE</b> .....	<b>20</b>
4.1 MEMORY MAP .....	20
4.2 DEFINITION OF PORT PINS .....	21
4.2.1 <i>Definition of DSP Port Pins</i> .....	21
4.3 INTERRUPT STRUCTURE.....	22
4.4 REGISTER.....	23
4.4.1 <i>Register Overview</i> .....	23
4.4.2 <i>PCB / Release Revision Register</i> .....	24
4.4.3 <i>TSI Control Register</i> .....	25
4.4.4 <i>Interrupt TSI Status/Clear Register</i> .....	25
4.4.5 <i>Interrupt TSI Mask Register</i> .....	26
4.4.6 <i>Interrupt DSP Status Register</i> .....	27
4.4.7 <i>Interrupt DSP Mask Register</i> .....	28
4.4.8 <i>DSP PLL/Reset Register</i> .....	29




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4.4.9	DSP Boot/Core-PLL Configuration .....	30
4.4.10	DSP Interrupt trigger Register .....	31
4.4.11	LED Control Register .....	32
4.5	FRONT PANEL AND LEDS .....	33
<b>5</b>	<b>CONNECTORS .....</b>	<b>34</b>
5.1	CONNECTOR OVERVIEW .....	34
5.2	CONNECTOR JP1: LATTICE PLL PROGRAMMING PORT .....	34
5.3	CONNECTOR JP2: ALTERA FPGA PROGRAMMING PORT .....	35
5.4	CONNECTOR JP4: BDM DEBUG CONNECTOR .....	35
5.5	PMC CONNECTOR P11 .....	36
5.6	PMC CONNECTOR P12 .....	37
5.7	PMC CONNECTOR P13 .....	38
5.8	PMC CONNECTOR P14 .....	39
<b>6</b>	<b>SOLDER FIELDS .....</b>	<b>40</b>
6.1	SOLDER FIELDS OVERVIEW .....	40
6.2	SOLDER FIELDS DESCRIPTION .....	41
<b>7</b>	<b>NPMC-DSP SETUP NOTES .....</b>	<b>42</b>
7.1	DSP BOOT MODE SETUP .....	42
7.2	DSP CORE-PLL CONFIGURATION WORD .....	42
<b>8</b>	<b>KNOWN BUGS / RESTRICTIONS .....</b>	<b>43</b>
	<b>APPENDIX A: REFERENCE DOCUMENTATION .....</b>	<b>44</b>
	<b>APPENDIX B: DOCUMENT'S HISTORY .....</b>	<b>45</b>

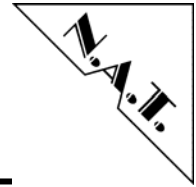


## List of Figures

Figure 1:	NPMC-DSP on a Carrier Board (VMEbus, cPCI).....	8
Figure 2:	NPMC-DSP Block Diagram .....	9
Figure 3:	Location Diagram of the NPMC-DSP .....	15
Figure 4:	Functional Block Diagram of the ADSP-BF535.....	16
Figure 5:	Local TDM Bus Organisation and Synchronisation .....	18
Figure 6:	Front Panel and LEDs .....	33
Figure 7:	Connectors of the NPMC-DSP .....	34
Figure 8:	Solder Fields of the NPMC-DSP .....	40

## List of Tables

Table 1:	List of used Abbreviations .....	7
Table 2:	NPMC-DSP Features .....	11
Table 3:	TDM Channel $\leftrightarrow$ DSP Serial Data Line Connection.....	19
Table 4:	Memory Map.....	20
Table 5:	DSP Port Pin Usage.....	21
Table 6:	Register Overview.....	23
Table 7:	PCB / FPGA Revision Register .....	24
Table 8:	Interrupt TSI Status/Clear Register .....	25
Table 9:	Interrupt TSI Mask Register.....	26
Table 10:	Interrupt DSP Status Register .....	27
Table 11:	Interrupt DSP Mask Register .....	28
Table 12:	DSP PLL/Reset Register .....	29
Table 13:	DSP PLL/Reset Register .....	30
Table 14:	DSP Interrupt trigger Register.....	31
Table 15:	LED Control Register.....	32
Table 16:	Lattice PLL Programming Port JP1 .....	34
Table 17:	Altera FPGA Programming Port JP2 .....	35
Table 18:	Development Port / BDM Connector Pinout JP4.....	35
Table 19:	PMC Connector P11.....	36
Table 20:	PMC Connector P12.....	37
Table 21:	PMC Connector P13.....	38
Table 22:	PMC Connector P14.....	39
Table 23:	Solder Fields and Related DSP FLASH / EEPROM Memories .....	41
Table 24:	DSP Boot Mode Configuration Word (as read from FPGA).....	42
Table 25:	DSP Core-PLL Configuration Word (as read from FPGA).....	42



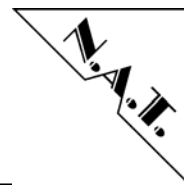
## Conventions

If not otherwise specified, addresses and memory maps are written in hexadecimal notation, identified by *0x*.

Table 1 gives a list of the abbreviations used in this document:

**Table 1: List of used Abbreviations**

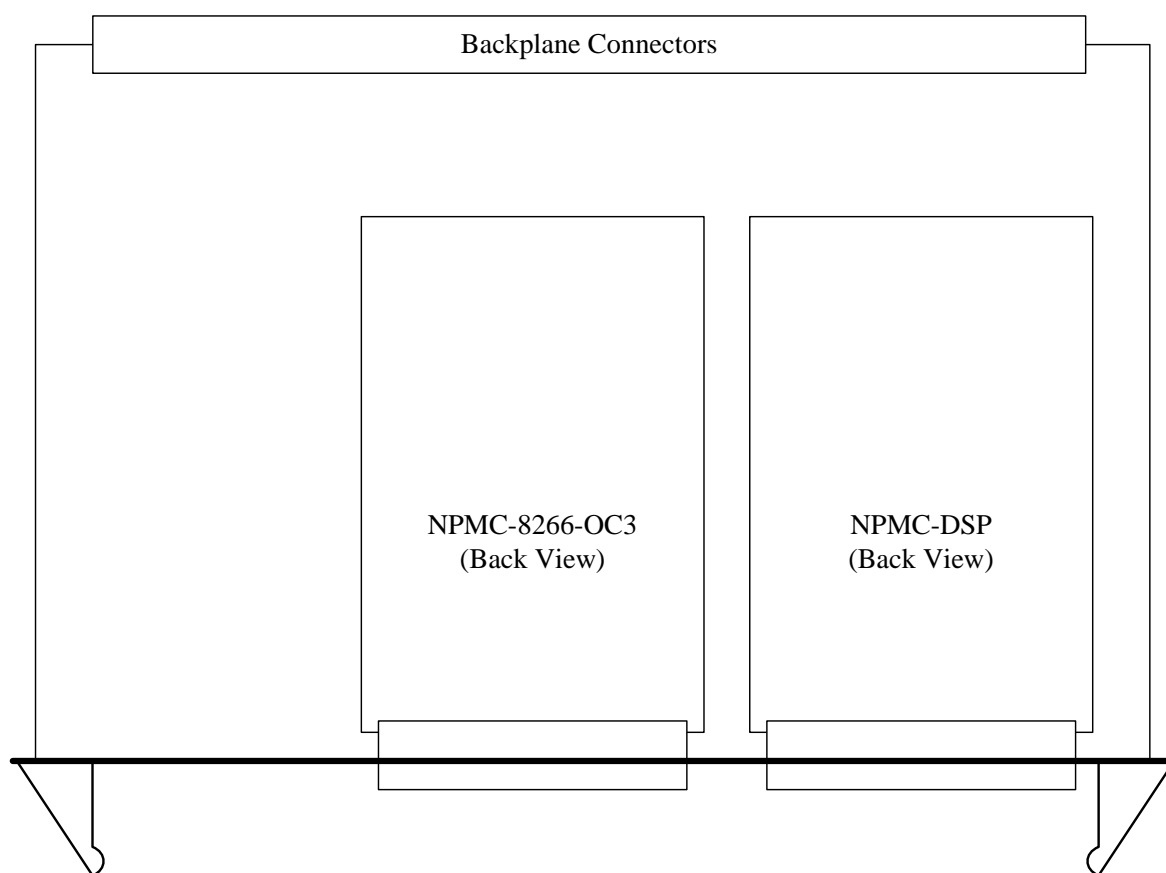
Abbreviation	Description
b	Bit, binary
B	byte
CPU	Central Processing Unit
DMA	Direct Memory Access
DSP	Digital Signal Processor
EEPROM	Electrically Erasable Programmable ROM
FLASH	Reprogrammable ROM
H.110	Time-Slot Interchange Bus
K	kilo (factor 400 in hex, factor 1024 in decimal)
M	mega (factor 10,000 in hex, factor 1,048,576 in decimal)
RAM	Random Access Memory
ROM	Read Only Memory
SCbus	Time-Slot Interchange Bus of the SCSA, subset of H.110 bus
SCSA	Signal Computing System Architecture
SDRAM	Synchronous Dynamic RAM
TDM	Time Division Multiplex
TSI	Time Slot Interchange
TSA	Time Slot Assigner

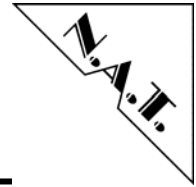


## 1 Introduction

The **NPMC-DSP** is a high performance standard CPU PCI Mezzanine Card Type 1. It can be plugged onto any carrier board supporting PMC standards:

**Figure 1: NPMC-DSP on a Carrier Board (VMEbus, cPCI)**

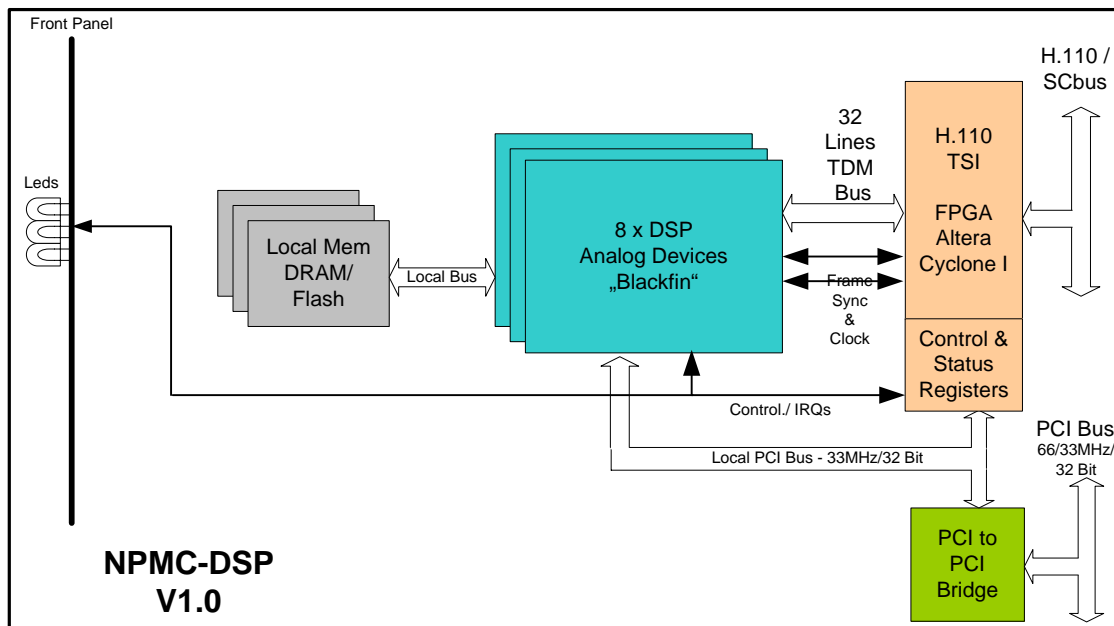


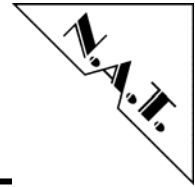


The **NPMC-DSP** has the following major features on-board:

- Blackfin Embedded Processor Architecture
- 32 bit / 66 MHz PCI Bus interface Rev. 2.2
- 8 x ADSP-BF535 signal processor
- Stratum 4 PLL
- H.110 / SCSA TSI bus
- SPI bus
- 8 x 32 MB main memory (SDRAM)
- 8 x 1 – 4 MB FLASH
- 8 x 32 kB Boot EEPROM

**Figure 2: NPMC-DSP Block Diagram**





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## 1.1 Board Features

- **DSPs**

Depending on the assembled version the Blackfin DSPs run with a core clock frequency of 300 - 350 MHz.

- **Memory**

**SDRAM:** The **NPMC-DSP** provides 32 MB local SDRAM for each DSP. The SDRAM is 32 bit wide.

**FLASH:** The **NPMC-DSP** provides local boot- and firmware FLASHes for each DSP. The SPI FLASH for storing firmware provides a capacity of 1 - 4 MB (assembly option). The SPI FLASH for boot code provides a capacity of 32kB.

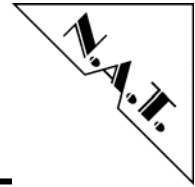
*Default:* 1 MB installed

- **Interfaces**

**PCI:** The **NPMC-DSP** includes a 32 bit 33/66 MHz PCI bus interface. This is implemented by a PLX PCI6150 bridging device.

**H.110/SCSA:** The **NPMC-DSP** implements a 32 bit H.110 interface, which includes a SCbus interface on I/O-connector P14 according to PMC specifications. This is implemented by an Altera Cyclone FPGA device. The H.110 interface is also available on PMC connector P13 according to PTMC configurations 3 and 5. PTID coding is configuration 5.

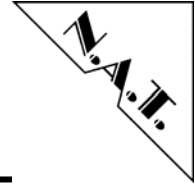
**SPI:** The **NPMC-DSP** implements a SPI bus interface on the PMC I/O connector P14, which connects to the Altera Cyclone FPGA.



## 1.2 Board Specification

**Table 2: NPMC-DSP Features**

Processor	8 x Blackfin ADSP-BF535 DSP (300 or 350 MHz)	
Board Format	Standard PCI Mezzanine Card Type 1	
Front-I/O	none	
Rear-I/O	H.110 and SCbus (32 bit) on P14, support of PTMC interface configurations 3 and 5 on P13. PTID coding is configuration 5.	
PCI to PMC bus bridge	PLX PCI 6150	
Main Memory	8 x 32 MByte SDRAM	
EEPROM	8 x 32 KByte EEPROM, on-board programmable	
FLASH PROM	8 x 1 – 4 MByte FLASH PROM, on-board programmable	
Firmware	BSP (on request)	
Power consumption with ADSP-BF535 DSP (300 MHz)	3.3V 0.8A typ. 5.0V 1.0A typ.	
Environmental conditions	Temperature (operating):	0°C to +60°C with forced cooling -40°C to +85°C
	Temperature (storage):	10 % to 90 % rh noncondensing
	Humidity:	
Standards compliance	PCI Rev. 2.2 IEEE P1386.1 / Draft 2.4a, PICMG 2.15 R1.0	



## 2 Installation

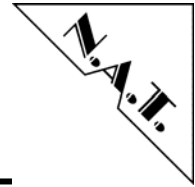
### 2.1 Safety Note

To ensure proper functioning of the **NPMC-DSP** during its usual lifetime take the following precautions before handling the board.

#### CAUTION

Electrostatic discharge and incorrect board installation and uninstallation can damage circuits or shorten their lifetime.

- Before installing or uninstalling the **NPMC-DSP** read this installation section
- Before installing or uninstalling the **NPMC-DSP**, read the Installation Guide and the User's Manual of the carrier board used
- Before installing or uninstalling the **NPMC-DSP** on a carrier board or both in a rack:
  - Check all installed boards and modules for steps that you have to take before turning on or off the power.
  - Take those steps.
  - Finally turn on or off the power.
- Before touching integrated circuits ensure to take all require precautions for handling electrostatic devices.
- Ensure that the **NPMC-DSP** is connected to the carrier board via all PMC connectors and that the power is available on both PMC connectors (GND, +5V, and +3,3V).
- When operating the board in areas of strong electromagnetic radiation ensure that the module
  - is bolted the front panel or rack
  - and shielded by closed housing



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## 2.2 Installation Prerequisites and Requirements

### IMPORTANT

Before powering up

- check this section for installation prerequisites and requirements

### 2.2.1 Requirements

The installation requires only

- a carrier board for connecting the **NPMC-DSP**
- power supply

### 2.2.2 Power supply

The power supply for the **NPMC-DSP** must meet the following specifications:

- required for the module:
  - +3,3V / 0.8A typical
  - +5,0V / 1.0A typical

### 2.2.3 Automatic Power Up

In the following situations the **NPMC-DSP** will automatically be reset and proceed with a normal power up.

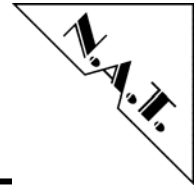
#### Voltage sensors

The voltage sensor generates a reset

- when +5V voltage level drops below 4,4V \*
- when +5V voltage level rises above 5,6V \*
- when +3.3V voltage level drops below 2,65V \*
- when +3.3V voltage level rises above 3,9V \*
- or when the carrier board signals a PCI Reset

#### Watchdog (if enabled)

\* defined by: “PCI Specification Revision 2.2, Section 4.2.1.1 and Section 4.3.2”



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## **2.3 Statement on Environmental Protection**

### **2.3.1 Compliance to RoHS Directive**

Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) predicts that all electrical and electronic equipment being put on the European market after June 30th, 2006 must contain lead, mercury, hexavalent chromium, polybrominated biphenyls (PBB) and polybrominated diphenyl ethers (PBDE) and cadmium in maximum concentration values of 0.1% respective 0.01% by weight in homogenous materials only.

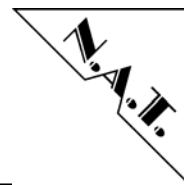
As these hazardous substances are currently used with semiconductors, plastics (i.e. semiconductor packages, connectors) and soldering tin any hardware product is affected by the RoHS directive if it does not belong to one of the groups of products exempted from the RoHS directive.

Although many of hardware products of N.A.T. are exempted from the RoHS directive it is a declared policy of N.A.T. to provide all products fully compliant to the RoHS directive as soon as possible. For this purpose since January 31st, 2005 N.A.T. is requesting RoHS compliant deliveries from its suppliers. Special attention and care has been paid to the production cycle, so that wherever and whenever possible RoHS components are used with N.A.T. hardware products already.

### **2.3.2 Compliance to WEEE Directive**

Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) predicts that every manufacturer of electrical and electronic equipment which is put on the European market has to contribute to the reuse, recycling and other forms of recovery of such waste so as to reduce disposal. Moreover this directive refers to the Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS).

Having its main focus on private persons and households using such electrical and electronic equipment the directive also affects business-to-business relationships. The directive is quite restrictive on how such waste of private persons and households has to be handled by the supplier/manufacturer, however, it allows a greater flexibility in business-to-business relationships. This pays tribute to the fact with industrial use electrical and electronic products are commonly integrated into larger and more complex environments or systems that cannot easily be split up again when it comes to their disposal at the end of their life cycles.



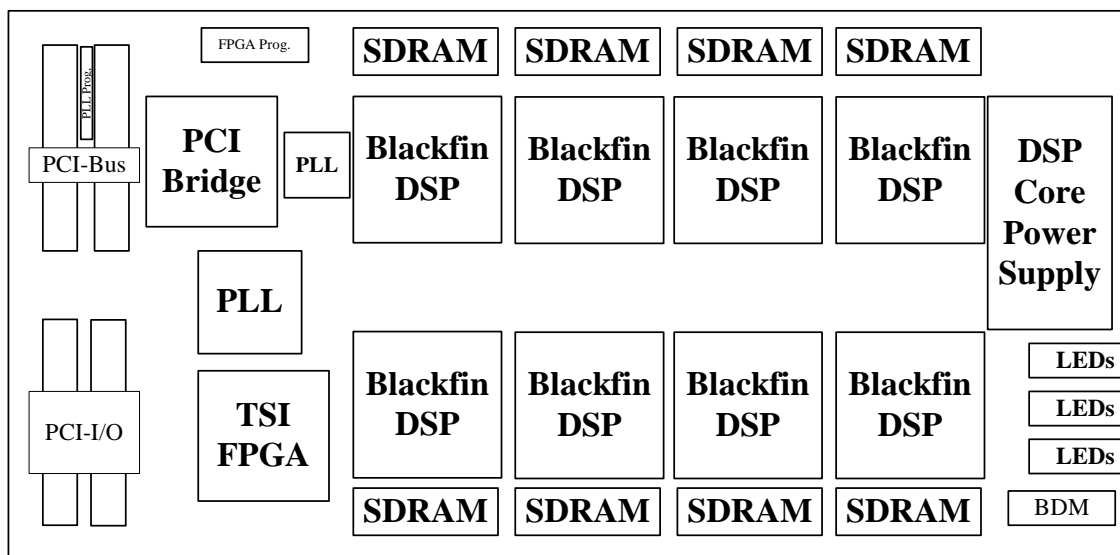
As N.A.T. products are solely sold to industrial customers, by special arrangement at time of purchase the customer agreed to take the responsibility for a WEEE compliant disposal of the used N.A.T. product. Moreover, all N.A.T. products are marked according to the directive with a crossed out bin to indicate that these products within the European Community must not be disposed with regular waste.

If you have any questions on the policy of N.A.T. regarding the Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) or the Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) please contact N.A.T. by phone or e-mail.

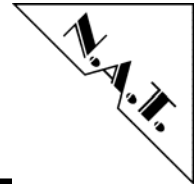
## 2.4 Location Overview

The figure 3 "Location diagram of the NPMC-DSP" highlights the position of the important components. Depending on the board type it might be that the board does not include all components named in the location diagram.

**Figure 3: Location Diagram of the NPMC-DSP**



Top View



### 3 Functional Blocks

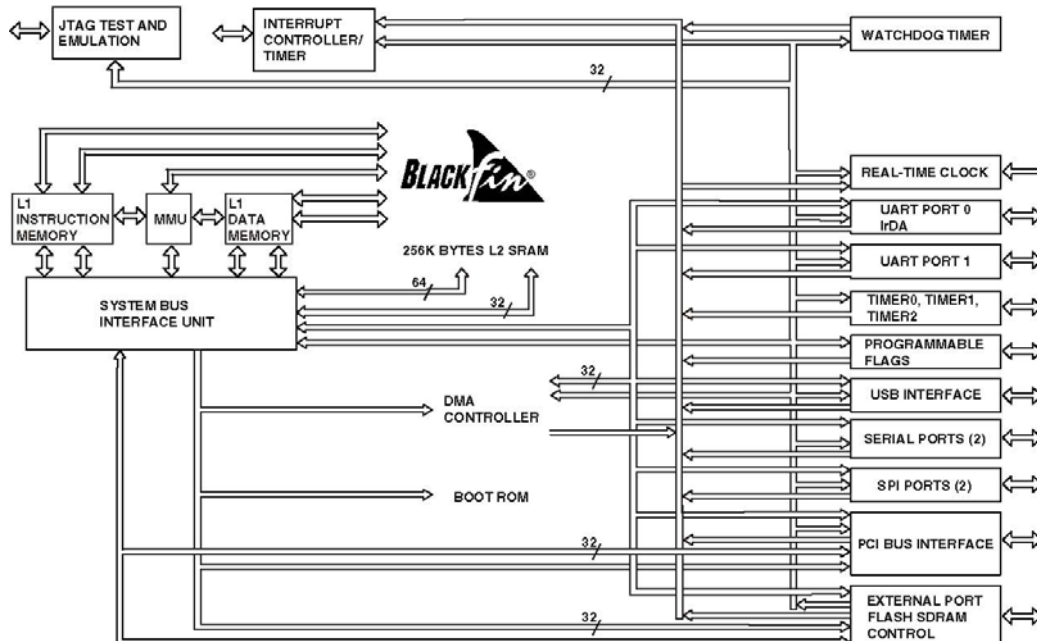
The **NPMC-DSP** can be divided into a number of functional blocks, which are described in the following paragraphs.

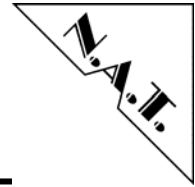
#### 3.1 DSPs

The ADSP-BF535 is a versatile signal processor that integrates on one chip a high-performance 350 MHz High Performance Blackfin Processor Core, a very flexible system integration unit, and many communications peripheral controllers that can be used in a variety of applications, particularly in communications and networking systems.

The core is an embedded variant of the Blackfin Processor Core with 16 KB of Instruction L1 SRAM/Cache, 32 KB of Data L1 SRAM/Cache, 4 KB of Scratch Pad L1 SRAM, 256 KB of L2 SRAM, a Memory DMA Controller, and a Memory Management Unit for memory protection. Furthermore it contains two 16-Bit MACs, two 40-Bit ALUs, a 40-Bit Shifter, four 8-Bit Video ALUs, and two 40-Bit Accumulators. The ADSP-BF535 can be accessed by the system through a 32-Bit, 33 MHz, PCI 2.2 Compliant Bus Interface with Master and Slave bus support. The system bus interface unit consists of a flexible memory controller that interfaces to almost any user-defined memory system, and many other peripherals making this device a complete system on a chip. These peripherals include two SPI Compatible Ports, two Full-Duplex Synchronous Serial Ports (SPORTs), four Timer/Counters, sixteen Bidirectional Programmable Flag I/O Pins, and a Watchdog Timer. Figure 4: shows a functional block diagram of the ADSP-BF535.

**Figure 4: Functional Block Diagram of the ADSP-BF535**





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## 3.2 PCI Interface

The **NPMC-DSP** includes a 32 bit, 33/66 MHz PCI interface to connect to the carrier board. This is implemented by an PLX PCI6150 PCI → PCI bridge.

The **NPMC-DSP** implements an internal 32 bit / 33 MHz PCI bus. This internal PCI bus connects to the 8 DSPs, and to the FPGA device, which implements the TDM TSI and some control/status registers.

## 3.3 Memory

### 3.3.1 SDRAM

As the onboard SDRAM memories have to be accessed not only by the DSPs, but also by the host through the PCI bridge, the DSP's PCI interfaces contain a FIFO structure to enable the user to access devices on the DSP's local bus. The SDRAMs are connected to the local bus interface of the DSPs. Every DSP has its own SDRAM on its own local bus. Hence, no bus arbitration is needed to access memory devices.

### 3.3.2 FLASH

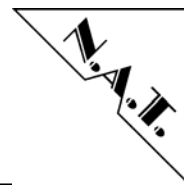
FLASH memory is connected to the SPI bus 0 of the DSP. Every DSP has its own FLASH on its own local SPI bus. The **NPMC-DSP** provides a local firmware FLASH for each DSP. The SPI FLASH for storing firmware provides a capacity of 1 - 4 MB (assembly option). It is accessed by SPI select generated on port pin PF12 of the DSP. Please note that this EEPROM is addressed with a 24-bit address!

### 3.3.3 EEPROM

EEPROM memory is connected to the SPI bus 0 of the DSP. Every DSP has its own EEPROM on its own local SPI bus. The **NPMC-DSP** provides a local boot EEPROM for each DSP. The SPI EEPROM for boot code provides a capacity of 32 kB. It is accessed by SPI select generated on port pin PF10 of the DSP. This SPI select becomes active by default after Reset when SPI boot is selected (default on the **NPMC-DSP**). Please note that this EEPROM is addressed with a 16-bit address!

### 3.3.4 I<sup>2</sup>C Device

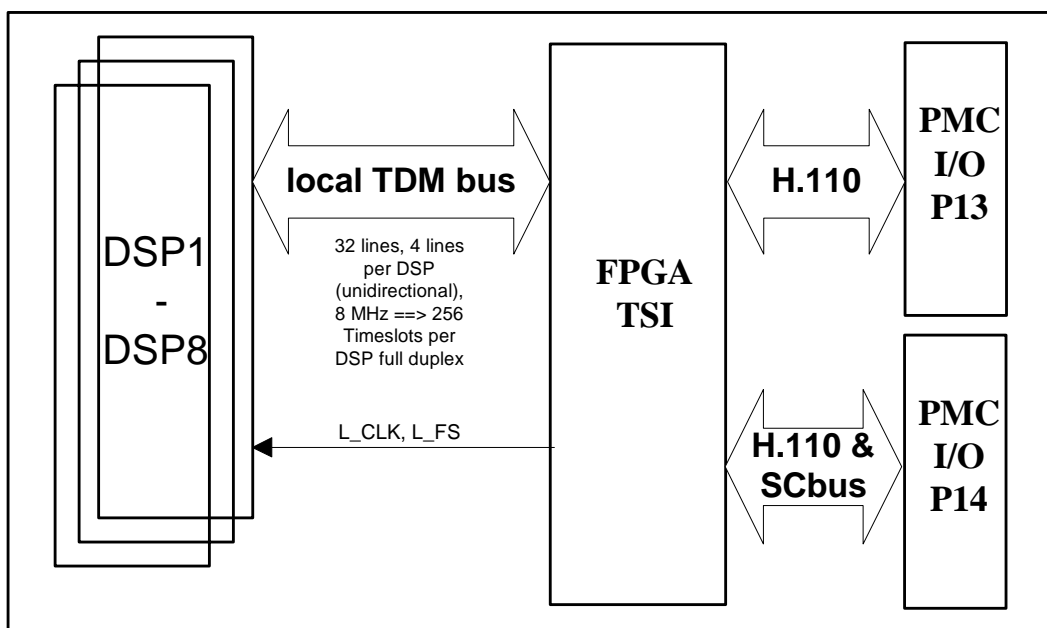
There is a I<sup>2</sup>C devices on the **NPMC-DSP**, which connects to the PCI6150 bridge device. This is used to provide the bridge with setup information after power-up. The address of the EEPROM is 0x0.



### 3.4 H.110 Bus Controller

#### 3.4.1 Block Diagramm of the TDM Structure

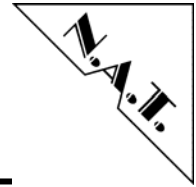
Figure 5: Local TDM Bus Organisation and Synchronisation



#### 3.4.2 Description of the TDM Structure

The TDM data are routed through the Altera Cyclone FPGA device, which implements a TSI device. Hence, any timeslot switching between H.110 bus and DSPs is possible. Local TDM data lines TDM[0 – 31] are routed between the DSPs and the TSI. The TSI device derives its time base from the H.110 bus. From this input it generates local clock and frame sync for the DSPs to synchronize to. Hence, the TSI implemented in the FPGA is always clock slave to the H.110 or SCbus on the carrier module. The Sync and Clock signals L\_FS and L\_CLK can be programmed within the FPGA control register settings.

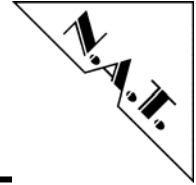
The connection between the TDM data lines TDM[0 – 31] and the corresponding serial channels DRx/DTx of the DSPs is shown in the following Table 3:


**Table 3: TDM Channel  $\leftrightarrow$  DSP Serial Data Line Connection**

<b>TSI local TDM Channel</b>	<b>DSP serial channel</b>	<b>TSI local TDM Channel</b>	<b>DSP serial channel</b>
TDM0	DSP1 DR0	TDM16	DSP5 DR0
TDM1	DSP1 DT0	TDM17	DSP5 DT0
TDM2	DSP1 DR1	TDM18	DSP5 DR1
TDM3	DSP1 DT1	TDM19	DSP5 DT1
TDM4	DSP2 DR0	TDM20	DSP6 DR0
TDM5	DSP2 DT0	TDM21	DSP6 DT0
TDM6	DSP2 DR1	TDM22	DSP6 DR1
TDM7	DSP2 DT1	TDM23	DSP6 DT1
TDM8	DSP3 DR0	TDM24	DSP7 DR0
TDM9	DSP3 DT0	TDM25	DSP7 DT0
TDM10	DSP3 DR1	TDM26	DSP7 DR1
TDM11	DSP3 DT1	TDM27	DSP7 DT1
TDM12	DSP4 DR0	TDM28	DSP8 DR0
TDM13	DSP4 DT0	TDM29	DSP8 DT0
TDM14	DSP4 DR1	TDM30	DSP8 DR1
TDM15	DSP4 DT1	TDM31	DSP8 DT1

### 3.4.3 SCbus Compatibility

The SCbus implemented on the **NPMC-DSP** is a sub-set of the H.110 bus. SCbus data lines correspond to H.110 data lines CT\_D[0 – 15]. On the **NPMC-DSP**, the bus width has been extended to 32 bit, in order to make use of all the 32 data lines switching capabilities of the TSI device. See Table 22: (PMC P14 Connector) for reference.



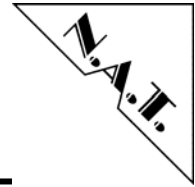
## 4 Hardware

### 4.1 Memory Map

Addresses are defined by programming the base and translation address registers which reside in the PCI configuration space of the PLX PCI6150 PCI bridge. This setting may be done by the user application-specific. Typically, 2 windows will be programmed, one to address the DSPs (which is subdivided by programming the base address registers in the PCI configuration space of the DSPs), and the other to address the TSI FPGA. Hence, the table below shows just a common example, which may be altered depending on the user's needs.

**Table 4: Memory Map**

Device	Address Offset	Function
DSP 1	0x0	DSP register access, FIFO window to local memory space
DSP 2	0x0010.0000	
DSP 3	0x0020.0000	
DSP 4	0x0030.0000	
DSP 5	0x0040.0000	
DSP 6	0x0050.0000	
DSP 7	0x0060.0000	
DSP 8	0x0070.0000	
TSI FPGA	0x0080.0000	TSI FPGA register access, routing memory



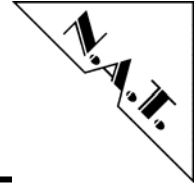
## 4.2 Definition of Port Pins

### 4.2.1 Definition of DSP Port Pins

FPGA pins are used to communicate with the DSP ports and to set up some board configuration. In detail:

**Table 5: DSP Port Pin Usage**

Port	Name	Description
PF0	PF0/SPISS0/MSEL0	PLL Configuration during Reset, prog. Flag, SPI Slave, SPI channel 0
PF1	PF1/SPISS1/MSEL1	PLL Configuration during Reset, prog. Flag, SPI Slave, SPI channel 1
PF2	PF2/SPI0SEL1/MSEL2	PLL Configuration during Reset, prog. Flag, SPI Master, SPI channel 0
PF3	PF3/SPI1SEL1/MSEL3	PLL Configuration during Reset, prog. Flag, SPI Master, SPI channel 1
PF4	PF4/SPI0SEL2/MSEL4	PLL Configuration during Reset, prog. Flag, SPI Master, SPI channel 0
PF5	PF5/SPI1SEL2/MSEL5	PLL Configuration during Reset, prog. Flag, SPI Master, SPI channel 1
PF6	PF6/SPI0SEL3/MSEL6	PLL Configuration during Reset, prog. Flag, SPI Master, SPI channel 0
PF7	PF7/SPI1SEL3/DF	PLL Configuration during Reset, prog. Flag, SPI Master, SPI channel 1
PF8	PF8/SPI0SEL4/SSEL0	PLL Configuration during Reset, prog. Flag, SPI Master, SPI channel 0
PF9	PF9/SPI1SEL4/SSEL1	PLL Configuration during Reset, prog. Flag, SPI Master, SPI channel 1
PF10	PF10/SPI0SEL5	prog. Flag, SPI Master, SPI channel 0 (default SPISEL after Reset), connected to Boot EEPROM
PF11	PF11/SPI1SEL5	prog. Flag, SPI Master, SPI channel 1, used as Interrupt Input (set by the TSI FPGA)
PF12	PF12/SPI0SEL6	prog. Flag, SPI Master, SPI channel 0, connected to Firmware FLASH
PF13	PF13/SPI1SEL6	prog. Flag, SPI Master, SPI channel 1, not used
PF14	PF14/SPI0SEL7	prog. Flag, SPI Master, SPI channel 0, not used
PF15	PF15/SPI1SEL7	prog. Flag, SPI Master, SPI channel 1, not used



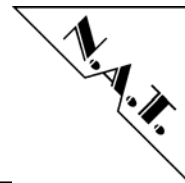
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### 4.3 *Interrupt Structure*

The **NPMC-DSP** has the following Interrupt structure:

Every DSP communicates interrupts to the TSI FPGA and vice versa through 2 interrupt pins. One of these (PCI /INTA) is used as interrupt output, thus signalling an interrupt request to the FPGA, the other (prog. Flag pin PF11) is used as interrupt input, thus is receiving interrupt requests from the FPGA. Please refer to the Interrupt Status Register in chapter 4.4.4, the Interrupt Mask Register in chapter 4.4.5, and the Interrupt Control Register in chapter 4.4.10 for details on how to set and mask these interrupts.

The FPGA may generate 2 different interrupt requests to the host, which are defined in the Interrupt Control Register. All 10 interrupt requests to the host, 2 from the TSI, and 8 from the DSPs, are wire-ored within the FPGA and fed to the /INTA signal of the PMC modules PCI interface, which connects to the carrier board.



## 4.4 Register

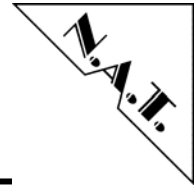
All registers described here are implemented in the FPGA TSI device. The base address is set within the PCI configuration space of the FPGA. The addresses given in the following paragraphs are offsets to this base address. Most registers are R/W and all are 16 bits wide by default.

### 4.4.1 Register Overview

The following table gives an overview of all registers contained in the Altera FPGA:

**Table 6: Register Overview**

Address	Reset Value	Name	Description
0x0000	0x1313	Version	Version Register
-	-	TSI_Control	Please refer to FPGA-TSI manual
0x1000	0x0000	IRQ_TSI_Stat	TSI interrupt status/clear
0x1002	0x0000	IRQ_TSI_Mask	TSI interrupt mask
0x1004	0x0000	IRQ_DSP_Stat	DSP interrupt status
0x1006	0x0000	IRQ_DSP_Mask	DSP interrupt mask
0x1200	0x0000	DSP_Res_PLL	DSP reset and external clock-PLL config
0x1202	0x0dac	DSP_Boot_Clock	DSP boot-mode and core/system clock config
0x1204	0x0000	DSP_Int	Trigger interrupt at the DSP's port-pin PF11
0x1206	0x0000	LED	Light/unlight LEDs

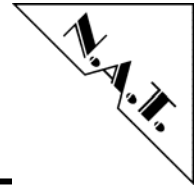


#### 4.4.2 PCB / Release Revision Register

There is a PCB / FPGA Revision Register implemented in the FPGA onboard the **NPMC-DSP**, which contains the revision code of the PCB, and the revision of the FPGA release. This code reads decimally-coded in 2 nibbles, i.e. the PCB version V1.0 reads 0x10. The register is addressed with address offset 0x0.

**Table 7: PCB / FPGA Revision Register**

Bit Number	Read/Write	Status Information / Control Setting
Bit 15	R	PCB Revision MSB
Bit 14	R	PCB Revision
Bit 13	R	PCB Revision
Bit 12	R	PCB Revision
Bit 11	R	PCB Revision
Bit 10	R	PCB Revision
Bit 9	R	PCB Revision
Bit 8	R	PCB Revision LSB
Bit 7	R	FPGA Revision MSB
Bit 6	R	FPGA Revision
Bit 5	R	FPGA Revision
Bit 4	R	FPGA Revision
Bit 3	R	FPGA Revision
Bit 2	R	FPGA Revision
Bit 1	R	FPGA Revision
Bit 0	R	FPGA Revision LSB



#### 4.4.3 TSI Control Register

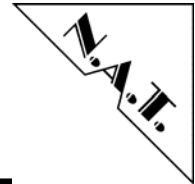
For the Registers controlling the TSI and settingup Time-Slot connections please contact N.A.T. for the FPGA-TSI manual.

#### 4.4.4 Interrupt TSI Status/Clear Register

This register is used to show the status of the internal interrupt sources of the TSI FPGA as well as to the common PCI-interrupt line. The register is addressed with address offset 0x1000. The TSI interrupts can be cleared by writing a '1' to the corresponding bit.

**Table 8: Interrupt TSI Status/Clear Register**

Bit Number	Read/Write	Default Value after Power-Up	Status Information / Control Setting
Bit 15	R	0	Common PCI-IRQ Status (1 = pending)
Bit 14	R	0	not used
Bit 13	R	0	not used
Bit 12	R	0	not used
Bit 11	R	0	not used
Bit 10	R	0	not used
Bit 9	R	0	not used
Bit 8	R	0	not used
Bit 7	R	0	not used
Bit 6	R	0	not used
Bit 5	R	0	not used
Bit 4	R	0	not used
Bit 3	R	0	not used
Bit 2	R	0	not used
Bit 1	w2c	0	TSI IRQ 1 (1 = pending)
Bit 0	w2c	0	TSI IRQ 0 (1 = pending)

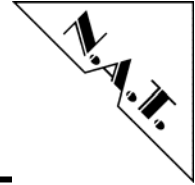


#### 4.4.5 Interrupt TSI Mask Register

This register is used to mask the internal interrupt sources of the TSI FPGA. The register is addressed with address offset 0x1002.

**Table 9: Interrupt TSI Mask Register**

Bit Number	Read/Write	Default Value after Power-Up	Status Information / Control Setting
Bit 15	R/W	0	not used
Bit 14	R/W	0	not used
Bit 13	R/W	0	not used
Bit 12	R/W	0	not used
Bit 11	R/W	0	not used
Bit 10	R/W	0	not used
Bit 9	R/W	0	not used
Bit 8	R/W	0	not used
Bit 7	R/W	0	not used
Bit 6	R/W	0	not used
Bit 5	R/W	0	not used
Bit 4	R/W	0	not used
Bit 3	R/W	0	not used
Bit 2	R/W	0	not used
Bit 1	R/W	0	TSI IRQ 1 Mask (1 = Int is active)
Bit 0	R/W	0	TSI IRQ 0 Mask (1 = Int is active)

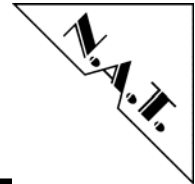


#### 4.4.6 Interrupt DSP Status Register

This register is used to show the status of the interrupt lines of the 8 DSPs. The register is addressed with address offset 0x1004.

**Table 10: Interrupt DSP Status Register**

Bit Number	Read/Write	Default Value after Power-Up	Status Information / Control Setting
Bit 15	R	0	not used
Bit 14	R	0	not used
Bit 13	R	0	not used
Bit 12	R	0	not used
Bit 11	R	0	not used
Bit 10	R	0	not used
Bit 9	R	0	not used
Bit 8	R	0	not used
Bit 7	R	0	DSP8 IRQ (1 = pending)
Bit 6	R	0	DSP7 IRQ (1 = pending)
Bit 5	R	0	DSP6 IRQ (1 = pending)
Bit 4	R	0	DSP5 IRQ (1 = pending)
Bit 3	R	0	DSP4 IRQ (1 = pending)
Bit 2	R	0	DSP3 IRQ (1 = pending)
Bit 1	R	0	DSP2 IRQ (1 = pending)
Bit 0	R	0	DSP1 IRQ (1 = pending)

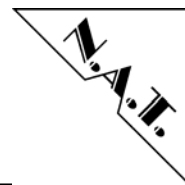


**4.4.7 Interrupt DSP Mask Register**

This register is used to mask the interrupt lines of the 8 DSPs. The register is addressed with address offset 0x1006.

**Table 11: Interrupt DSP Mask Register**

Bit Number	Read/Write	Default Value after Power-Up	Status Information / Control Setting
Bit 15	R/W	0	not used
Bit 14	R/W	0	not used
Bit 13	R/W	0	not used
Bit 12	R/W	0	not used
Bit 11	R/W	0	not used
Bit 10	R/W	0	not used
Bit 9	R/W	0	not used
Bit 8	R/W	0	not used
Bit 7	R/W	0	DSP8 IRQ Mask (1 = Int is active)
Bit 6	R/W	0	DSP7 IRQ Mask (1 = Int is active)
Bit 5	R/W	0	DSP6 IRQ Mask (1 = Int is active)
Bit 4	R/W	0	DSP5 IRQ Mask (1 = Int is active)
Bit 3	R/W	0	DSP4 IRQ Mask (1 = Int is active)
Bit 2	R/W	0	DSP3 IRQ Mask (1 = Int is active)
Bit 1	R/W	0	DSP2 IRQ Mask (1 = Int is active)
Bit 0	R/W	0	DSP1 IRQ Mask (1 = Int is active)

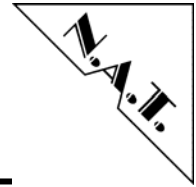


#### 4.4.8 DSP PLL/Reset Register

This register is used to setup the configuration for the PLL sourcing the DSP's core clock, and to reset some or all of the DSPs. Currently the only supported PLL configuration is "00". A DSP can be reset by setting the corresponding bit to '1'. The register is addressed with address offset 0x1200.

**Table 12: DSP PLL/Reset Register**

Bit Number	Read/Write	Default Value after Power-Up	Status Information / Control Setting
Bit 15	R/W	0	not used
Bit 14	R/W	0	not used
Bit 13	R/W	0	not used
Bit 12	R/W	0	not used
Bit 11	R/W	0	not used
Bit 10	R/W	0	not used
Bit 9	R/W	0	DSP_PLL_DS1
Bit 8	R/W	0	DSP_PLL_DS0
Bit 7	R/W	0	RES_DSP8 (1 = assert reset)
Bit 6	R/W	0	RES_DSP7 (1 = assert reset)
Bit 5	R/W	0	RES_DSP6 (1 = assert reset)
Bit 4	R/W	0	RES_DSP5 (1 = assert reset)
Bit 3	R/W	0	RES_DSP4 (1 = assert reset)
Bit 2	R/W	0	RES_DSP3 (1 = assert reset)
Bit 1	R/W	0	RES_DSP2 (1 = assert reset)
Bit 0	R/W	0	RES_DSP1 (1 = assert reset)



#### 4.4.9 DSP Boot/Core-PLL Configuration

This register is used to setup the configuration for the DSP's boot mode, and to select the core- and system-clock frequency of the DSPs. The current configuration results in booting from SPI-flash-memory, and in core/system clock frequencies of 300/120 MHz. Changes to this register become active after asserting a reset to the DSPs.

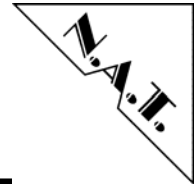
Be careful not to exceed the maximum values for the DSP's core/system clock!

Please refer to chapter 7 for additional information.

The register is addressed with address offset 0x1202.

**Table 13: DSP PLL/Reset Register**

Bit Number	Read/Write	Default Value after Power-Up	Status Information / Control Setting
Bit 15	R/W	0	not used
Bit 14	R/W	0	not used
Bit 13	R/W	0	not used
Bit 12	R/W	0	BMODE 2
Bit 11	R/W	1	BMODE 1
Bit 10	R/W	1	BMODE 0
Bit 9	R/W	0	PF 9
Bit 8	R/W	1	PF 8
Bit 7	R/W	1	PF 7
Bit 6	R/W	0	PF 6
Bit 5	R/W	1	PF 5
Bit 4	R/W	0	PF 4
Bit 3	R/W	1	PF 3
Bit 2	R/W	1	PF 2
Bit 1	R/W	0	PF 1
Bit 0	R/W	0	PF 0

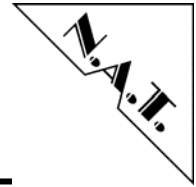


**4.4.10 DSP Interrupt trigger Register**

This register is used to set interrupts at the PF11 prog. Flag pins of the 8 DSPs. The register is addressed with address offset 0x1204.

**Table 14: DSP Interrupt trigger Register**

Bit Number	Read/Write	Default Value after Power-Up	Status Information / Control Setting
Bit 15	R/W	0	not used
Bit 14	R/W	0	not used
Bit 13	R/W	0	not used
Bit 12	R/W	0	not used
Bit 11	R/W	0	not used
Bit 10	R/W	0	not used
Bit 9	R/W	0	not used
Bit 8	R/W	0	not used
Bit 7	R/W	0	IRQ to DSP8 on PF11 prog. Flag pin
Bit 6	R/W	0	IRQ to DSP7 on PF11 prog. Flag pin
Bit 5	R/W	0	IRQ to DSP6 on PF11 prog. Flag pin
Bit 4	R/W	0	IRQ to DSP5 on PF11 prog. Flag pin
Bit 3	R/W	0	IRQ to DSP4 on PF11 prog. Flag pin
Bit 2	R/W	0	IRQ to DSP3 on PF11 prog. Flag pin
Bit 1	R/W	0	IRQ to DSP2 on PF11 prog. Flag pin
Bit 0	R/W	0	IRQ to DSP1 on PF11 prog. Flag pin

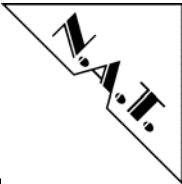


#### 4.4.11 LED Control Register

This register is used to control the 12 front-panel LEDs. A LED is lighted if the corresponding bit is set to '1'. The register is addressed with address offset 0x1206.

**Table 15: LED Control Register**

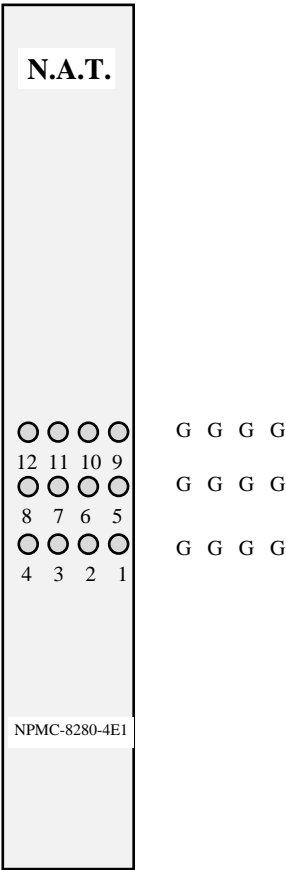
Bit Number	Read/Write	Default Value after Power-Up	Status Information / Control Setting
Bit 15	R/W	0	not used
Bit 14	R/W	0	not used
Bit 13	R/W	0	not used
Bit 12	R/W	0	not used
Bit 11	R/W	0	LED12 (1 = LED lighted)
Bit 10	R/W	0	LED11 (1 = LED lighted)
Bit 9	R/W	0	LED10 (1 = LED lighted)
Bit 8	R/W	0	LED9 (1 = LED lighted)
Bit 7	R/W	0	LED8 (1 = LED lighted)
Bit 6	R/W	0	LED7 (1 = LED lighted)
Bit 5	R/W	0	LED6 (1 = LED lighted)
Bit 4	R/W	0	LED5 (1 = LED lighted)
Bit 3	R/W	0	LED4 (1 = LED lighted)
Bit 2	R/W	0	LED3 (1 = LED lighted)
Bit 1	R/W	0	LED2 (1 = LED lighted)
Bit 0	R/W	0	LED1 (1 = LED lighted)



### 4.5 Front Panel and LEDs

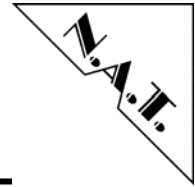
The NPMC-DSP module is equipped with 12 LEDs, which are software programmable. Thus their functionality depends very much on the application running on the module.

Figure 6: Front Panel and LEDs



**LEDs:**

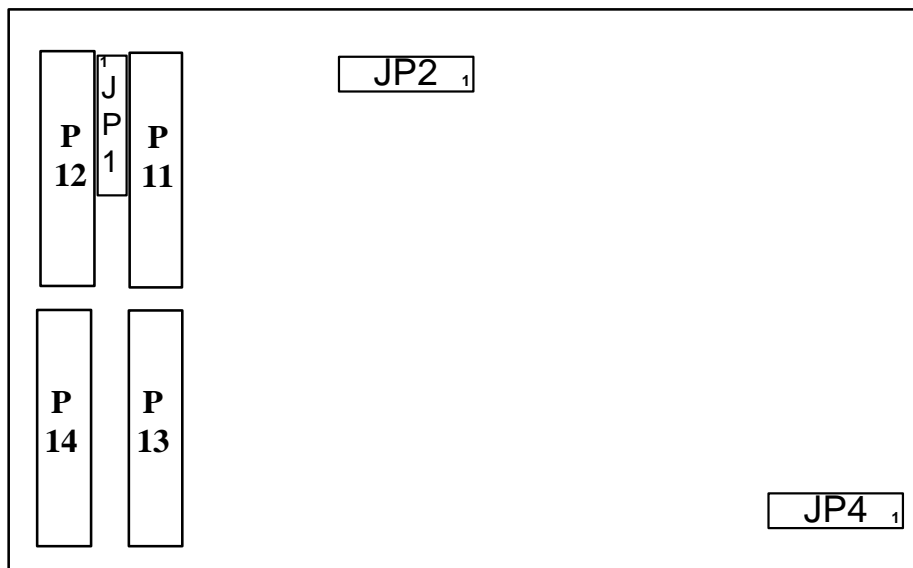
LED 12 - 1 the green LEDs 12 – 1 are fully software programmable and their meaning depends on user application.



## 5 Connectors

### 5.1 Connector Overview

Figure 7: Connectors of the NPMC-DSP



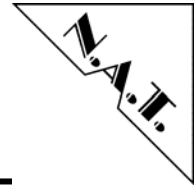
Please refer to the following tables to look up the pin assignment of the **NPMC-DSP** connectors.

### 5.2 Connector JP1: Lattice PLL Programming Port

Connector JP1 connects the JTAG- or programming port of the Lattice PLL device.

Table 16: Lattice PLL Programming Port JP1

Pin No.	Signal	Signal	Pin No.
1	TCK	nc	2
3	TMS	GND	4
5	TDI	+3.3V	6
7	TDO	GND	8
9	nc	nc	10



### 5.3 Connector JP2: Altera FPGA Programming Port

Connector JP2 connects the programming port of the Altera serial PROM device used for loading the Cyclone FPGA.

**Table 17: Altera FPGA Programming Port JP2**

Pin No.	Signal	Signal	Pin No.
1	DCLK	GND	2
3	CONF_DONE	+3.3V	4
5	/CONFIG	/CECONF	6
7	DATA0	/CS0	8
9	ASDI	GND	10

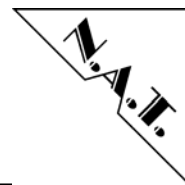
### 5.4 Connector JP4: BDM Debug Connector

Connector JP4 connects the JTAG / development Port / BDM Port of the DSPs. The DSPs form a daisy chain, with DSP1 being the first, and DSP8 being the last in the chain.

**Table 18: Development Port / BDM Connector Pinout JP4**

Pin No.	Signal	Signal	Pin No.
1	TCK	GND	2
3	TMS	+3.3V	4
5	TDI	IO_SENSE	6
7	TDO	/EMU	8
9	/TRST	GND	10

The BDM port (also called COP header) can be used for debugging. It is supported by major debug tool manufacturers.

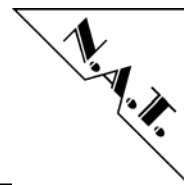


## 5.5 PMC Connector P11

Table 19: PMC Connector P11

Pin No.	PCI-Signal	PCI-Signal	Pin No.
1	TCK	-12V	2
3	GND	/INT A	4
5	/INT B	/INT C	6
7	/BUSMODE1	+5V	8
9	/INT D	PCI_RSV1	10
11	GND	3.3Vaux	12
13	CLK	GND	14
15	GND	/GNT	16
17	/REQ	+5V	18
19	V (I/O)	AD31	20
21	AD28	AD22	22
23	AD25	GND	24
25	GND	CBE3	26
27	AD22	AD21	28
29	AD19	+5V	30
31	V (I/O)	AD17	32
33	/FRAME	GND	34
35	GND	/IRDY	36
37	/DEVSEL	+5V	38
39	GND	/LOCK	40
41	/SDONE	/SB0	42
43	PAR	GND	44
45	V (I/O)	AD15	46
47	AD12	AD11	48
49	AD09	+5V	50
51	GND	/CBE0	52
53	AD06	AD05	54
55	AD04	GND	56
57	V (I/O)	AD03	58
59	AD02	AD01	60
61	AD00	+5V	62
63	GND	/REQ64	64

Pins for –12V, and Vaux are not connected to the module. The same applies to JTAG signal TCK and PCI signals /LOCK, /REQ64, /SDONE, /SBO, /INTB, /INTC, /INTD. The PCI bridge chip always drives signals to 3.3V level, but it 5V tolerant.

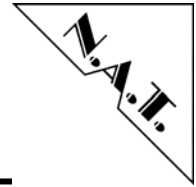


## 5.6 PMC Connector P12

Table 20: PMC Connector P12

Pin No.	PCI-Signal	PCI-Signal	Pin No.
1	+12V	/TRST	2
3	TMS	TDO	4
5	TDI	GND	6
7	GND	PCI_RSV3	8
9	PCI_RSV	PCI_RSV4	10
11	/BUSMODE2	+3.3V	12
13	/PCIRST	/BUSMODE3	14
15	+3.3V	/BUSMODE4	16
17	/PME	GND	18
19	AD30	AD29	20
21	GND	AD26	22
23	AD24	+3.3V	24
25	IDSEL	AD23	26
27	+3.3V	AD20	28
29	AD18	GND	30
31	AD16	/CBE2	32
33	GND	PCI_RESVD	34
35	/TRDY	+3.3V	36
37	GND	/STOP	38
39	/PERR	GND	40
41	+3.3V	/SERR	42
43	/CBE1	GND	44
45	AD14	AD13	46
47	M66EN	AD10	48
49	AD08	+3.3V	50
51	AD07	PCI_RESV	52
53	+3.3V	PCI_RESV	54
55	PCI_RESV	GND	56
57	PCI_RESV	PCI_RESV	58
59	GND	PCI_RESV	60
61	ACK64	+3.3V	62
63	GND	PCI_RESV	64

Pins for +12V and /BUSMODE2 are not connected to the module. The same applies to /ACK64 and /PME, as well as to the JTAG signals TMS and /TRST. JTAG TDI is connected to TDO.

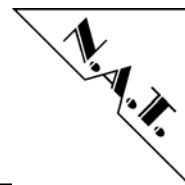


## 5.7 PMC Connector P13

Table 21: PMC Connector P13

Pin No.	PCI-Signal	PCI-Signal	Pin No.
1	CT_D26	GND	2
3	GND	NC	4
5	CT_D24	NC	6
7	CT_D22	GND	8
9	PTID2	CT_D31	10
11	GND	CT_D29	12
13	CT_D20	GND	14
15	GND	CT_D27	16
17	FRAME_A	CT_D25	18
19	FRAME_B	GND	20
21	PTID0	CT_D23	22
23	GND	CT_D21	24
25	CT_C8A	GND	26
27	GND	CT_D19	28
29	CT_D18	CT_D17	30
31	CT_D16	GND	32
33	GND	NETREF2	34
35	CT_D14	CT_D30	36
37	CT_D12	GND	38
39	PTENB	CT_D28	40
41	GND	NETREF1	42
43	CT_C8B	GND	44
45	GND	CT_D15	46
47	CT_D10	CT_D13	48
49	CT_D8	CT_D11	50
51	GND	CT_D9	52
53	CT_D7	CT_D6	54
55	CT_D4	GND	56
57	PTID1	CT_D5	58
59	CT_D2	CT_D3	60
61	CT_D0	GND	62
63	GND	CT_D1	64

The pinning and signal definition of PMC connector P13 conforms to the PTMC specification PICMG 2.15 R1.0, configuration 3 and 5. PTID coding is configuration 5.

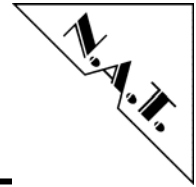


## 5.8 PMC Connector P14

Table 22: PMC Connector P14

Pin No.	PCI-Signal	PCI-Signal	Pin No.
1	MC	CT_D15	2
3	CT_D14	CT_D13	4
5	CT_D12	GND	6
7	CT_D11	CT_D10	8
9	CT_D09	CT_D8	10
11	CT_D07	GND	12
13	CT_D06	CT_D5	14
15	CT_D04	CT_D3	16
17	CT_D02	CT_D1	18
19	GND	CT_D0	20
21	NC	/FSYNC	22
23	SREF_8K	SCLK	24
25	GND	/SCLKx2	26
27	NC	NC	28
29	NC	NC	30
31	NC	NC	32
33	SPICLK	/SPISEL	34
35	SPIMISO	SPIMOSI	36
37	NC	FRAME_B	38
39	FRAME_A	NETREF2	40
41	NETREF1	NC	42
43	NC	GND	44
45	CT_C8_B	CT_C8_A	46
47	CT_D16	CT_D17	48
49	CT_D18	CT_D19	50
51	GND	CT_D20	52
53	CT_D21	CT_D22	54
55	CT_D23	CT_D24	56
57	GND	CT_D25	58
59	CT_D26	CT_D27	60
61	CT_D28	CT_D29	62
63	CT_D30	CT_D31	64

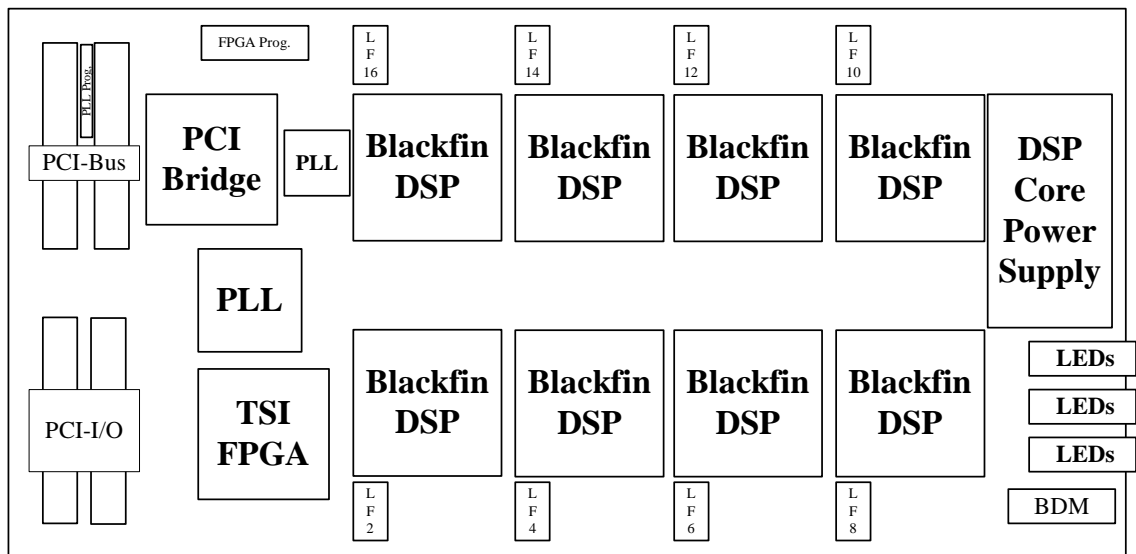
The pinning and signal definition of PMC connector P14 is similar to the draft version of VITA 36 (PMC IO Module Standard, as SCbus pin assignment is concerned. This refers to P14 pins 1 – 32. Pins 33 – 64 carry the 32-bit extension and control signals of H.110.



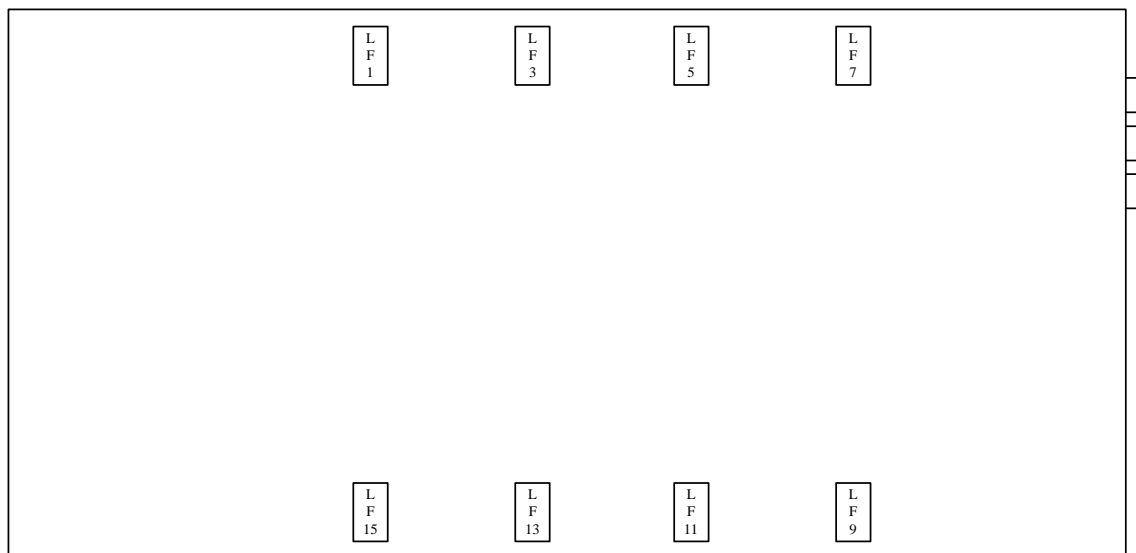
## 6 Solder Fields

### 6.1 Solder Fields Overview

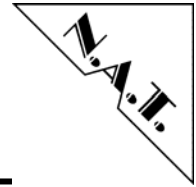
Figure 8: Solder Fields of the NPMC-DSP



Top View



Bottom View

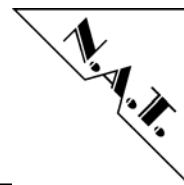


## 6.2 Solder Fields Description

There are 16 solder fields on the **NPMC-DSP**, which, when closed, may be used to write-protect the SPI EEPROMs and FLASHes connected to the 8 DSPs. Figure 8: shows the locations of these solderfields. They are related to the DSPs and their EEPROMs/FLASHes as follows:

**Table 23: Solder Fields and Related DSP FLASH / EEPROM Memories**

Solder Field	Related DSP	Memory Device, which is Write-Protected when Solder Field is closed
LF 1	DSP1	Boot EEPROM
LF 2	DSP1	Firmware FLASH
LF 3	DSP2	Boot EEPROM
LF 4	DSP2	Firmware FLASH
LF 5	DSP3	Boot EEPROM
LF 6	DSP3	Firmware FLASH
LF 7	DSP4	Boot EEPROM
LF 8	DSP4	Firmware FLASH
LF 9	DSP5	Boot EEPROM
LF 10	DSP5	Firmware FLASH
LF 11	DSP6	Boot EEPROM
LF 12	DSP6	Firmware FLASH
LF 13	DSP7	Boot EEPROM
LF 14	DSP7	Firmware FLASH
LF 15	DSP8	Boot EEPROM
LF 16	DSP8	Firmware FLASH



## 7 NPMC-DSP Setup Notes

### 7.1 DSP Boot Mode Setup

The basic setting of the boot mode is done by pulling the BMODE pins during /RESET. These are programmable through FPGA U35 (BMODE0-2). Alternative, the boot mode may be set by Pullup/Pulldown resistors. In this case the FPGA outputs to the BMODEx port pins have to be disabled. Default setting: resistors not installed, Boot Mode set by the FPGA. The default configuration word reads as follows:

**Table 24: DSP Boot Mode Configuration Word** (as read from FPGA)

Name	Value	Description
BMODE0	1b	Boot Mode Configuration during Reset
BMODE1	1b	``
BMODE2	0b	``

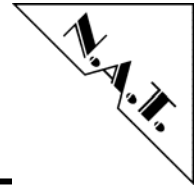
The default configuration boots from the 32 kB EEPROM, which is connected to Port PF10/SPISEL5, which is used as boot SPISEL by the DSP.

### 7.2 DSP Core-PLL Configuration Word

The ADSP BF535 DSPs read their configuration data during the /RESET - phase from the FPGA. Alternatively, this Configuration Word may be set by Pullup/Pulldown resistors. In this case the FPGA outputs to the PFx port pins have to be disabled. Default setting: resistors not installed, configuration word set by the FPGA. The default configuration (core-clock: 300MHz, system-clock: 120 MHz) word reads as follows:

**Table 25: DSP Core-PLL Configuration Word** (as read from FPGA)

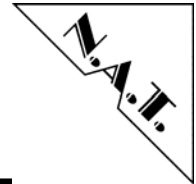
Port	Name	Value	Description
PF0	MSEL0	0b	PLL Configuration during Reset
PF1	MSEL1	0b	``
PF2	MSEL2	1b	``
PF3	MSEL3	1b	``
PF4	MSEL4	0b	``
PF5	MSEL5	1b	``
PF6	MSEL6	0b	``
PF7	DF	1b	``
PF8	SSEL0	1b	``
PF9	SSEL1	0b	PLL Configuration during Reset



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## 8 Known Bugs / Restrictions

none



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## Appendix A: Reference Documentation

- [1] Analog Devices, Blackfin Embedded Processor ADSP-BF535 Reference Manual, 2004, Rev. A
- [2] Altera Corp., Cyclone FPGA Family Data Sheet, Cyclone Device Handbook, Volume 1.2, 10/2003
- [3] Altera Corp., Cyclone Device Handbook, Volume 1.2, 10/2003
- [4] NexFlash Technologies Inc., spiflash data sheet, NXSF044E-0604, 7/2004
- [5] Micron Technologies, Inc., MT48LC8M32B2 Data Sheet, Rev. B, 10/2004
- [6] PLX Technology, PCI 6150 (HB4) PCI to PCI Bridge Data Book, Ver. 2.0, 5/2003
- [7] ZARLINK Semiconductor, ZL30100 E1/T1 System Synchronizer Data Sheet, 2/2005
- [8] Lattice Semiconductor Corp., ispCLOCK 5600 Family Data Sheet, 2/2005
- [9] tyco Electronics, Austin Lynx SMT non-isolated Power Modules, Data Sheet, 10/2002

