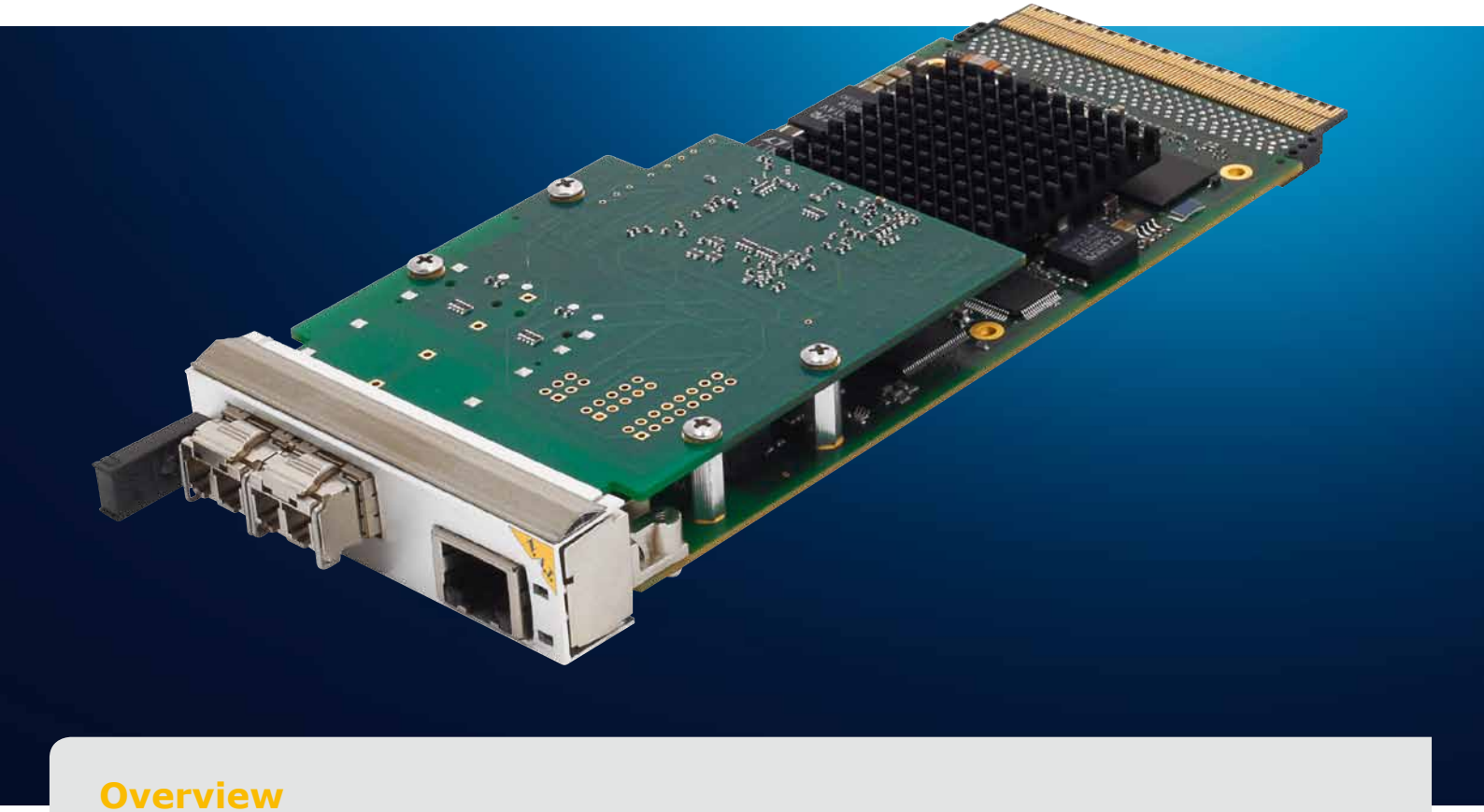
NAMC-8569-ATM



Overview

The **NAMC-8569-ATM** is a multi-service ATM board in Advanced Mezzanine Card (AMC) form factor featuring data exchange between optical OC3/STM1 ATM traffic. Flexibility, high-bandwidth and low latency processing dedicate the **NAMC-8569-ATM** for applications in telecommunication and defense communication market. The front Ethernet interface can be switched or multiplexed towards the CPU and the backplane. Depending on the required throughput one Fat Pipe (PCIe or SRIO) or the combination of both Fat Pipes (PCIe and SRIO) are available to the backplane. Thus, the **NAMC-8569-ATM** is targeting at ATM based applications where IO boards need PCIe and where low latency of SRIO for multiprocessing is requested.

Key features

- Latest Freescale™ PowerQUICC® III MPC8569 processor @1.33 GHz
  - dual Multichannel Communication
  - Controller (MCC)
  - higher core frequency than predecessor PowerQUICC III processors
- up to 1GB DDR2 SDRAM at 800MHz, 128MB Flash
- Lattice ECP3 FPGA
  - up to 70.000 logic cells
- Interfaces at front panel
  - 1x Gigabit Ethernet (GbE)
  - 2x OC3 SFP
- Backplane connections
  - 2x Gigabit Ethernet (GbE)
  - Serial Rapid IO (SRIO)
  - PCI Express (PCIe)
- TDM and I-TDM
  - 125 µs and 1 ms I-TDM modes as well as TDM cross-connect supported

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Technical Data
NAMC-8569-ATM

Overview

The **NAMC-8569-ATM** is a multi-service processor board featuring ATM, multiple Ethernet, SRIO, PCIe interfaces and optional TDM connectivity. It is available as a single width, mid- and full-size AMC. The AMC board provides flexibility, high-bandwidth and low latency processing in next generation systems based on the MicroTCA® or ATCA standards. The combination of software based processing resources and FPGA based hardware resources dedicate the **NAMC-8569-ATM** for a wide-spread of possible applications in telecommunication and defense&aerospace market.

ATM Interworking Support

The MPC8569's PowerQUICC Engine offers extensive interworking support between TDM/I-TDM (AAL1 Circuit Emulation Service CES) as well as Ethernet and ATM without CPU intervention. Lookup keys can be generated from Ethernet headers up to layer 4. The board supports header manipulation which is commonly used to perform Network Address Port Translation (NAPT). A further function is insertion and removal of bytes at user-specific offsets including checksum updates.

CPU and Memory

The **NAMC-8569-ATM** is equipped with the powerful Freescale PowerQUICC III MPC8569. It offers an e500 PowerPC core combined with dedicated interface hardware and four RISC cores. This network processor operates at core frequencies of 800MHz, 1.0 or 1.3GHz. The main on-board memory is a 128-1024 MB DDR2 SDRAM. In addition, the **NAMC-8569-ATM** is equipped with 16-128 MB 16-bit parallel FLASH (NOR) and 2GB NAND Flash memory. A Micro-SD-Card slot could be used for high capacity, non-volatile and removable memory. Permanent write capabilities, i.e. for data capturing, are provided by an optional 512 kB MRAM (non-volatile SRAM).

Front Panel Interfaces

The **NAMC-8569-ATM** is based on a rich offer of versatile interfaces for flexible deployment. The dual SFP based OC3 optical interfaces offer access to a wide range of ATM applications. The GbE interface is directly connected to the FPGA from Lattice and can be operated via back plane or front panel, or in a combination of both.

TDM and I-TDM Interface

The ECP3 FPGA from Lattice provides the powerful TDM to I-TDM bridge and a timeslot interchanger (TSI). The TDM-to-I-TDM bridge converts the TDM oriented bit stream into Ethernet packets and vice versa. In addition to the I-TDM interface, the TSI offers an optional 32MHz clocked H.110-alike TDM backplane interface at the AMC connector (extended area). Line interfaces of other AMC boards for example the NAMC-xE1/T1 can be directly connected to channels of the MPC8569 MCC controllers allowing flexible routing.

Fabric Support
Fat Pipe

The **NAMC-8569-ATM** offers four bidirectional serial lanes that can be operated either as PCIe, SRIO, or a combination of both.

The **NAMC-8569-ATM** can be configured to implement either PCIe: one x1 (port 4/8) or one x4 (ports 4-7/8-11). SRIO: two x1 (port 4 and 8) or one x4 (ports 4-7/8-11). The speed is configurable for 1.25 Gb/s, 2.5 Gb/s or 3.125 Gb/s. PCIe and SRIO: one x1 PCIe (port 4) and one SRIO (port 8). In this case the speed of the SRIO interface is fixed at 2.5 Gb/s.

Base Fabric

The **NAMC-8569-ATM** provides two 1000BaseX interfaces at port 0 and port 1 of the common options region of the AMC backplane connector.

Key Features

System Processor and Memory
- up to 1,3 GHz Freescale Power QUICCIII MPC8569
- 128-1024 MB DDR2 SDRAM
- 16-128 MB FLASH
- Micro-SD-Card slot
- 512 kB MRAM
- 2 GB NAND Flash

ATM Interworking Support
- Interworking capabilities I-TDM/TDM or Ethernet and ATM
- IP over ATM Routing & Forwarding
- ATM AAL0, AAL1, AAL2, AAL5

Front Panel Interfaces
- 1x GbE

Backplane Connectivity

Base Fabric
- 2x 1GbE at AMC port 0 and 1

Fat Pipe Interface Options
- PCIe x4 on ports 4-7 or 8-11
- PCIe x1 on port 4 or 8
- SRIO x4 on ports 4-7 or 8-11
- SRIO x1 on ports 4 and 8
- PCIe x1 on port 4 and SRIO x1 on port 8

I-TDM Interface
- 1024 bidirect. 64 kbit/s channels
- 125 µs-mode and 1ms-mode support

TDM (optional)
- H.110 alike 32MHz clocked TDM interface connects to ports 12, 13 (data) and port 14 (sync)

Indicator LEDs
- 2 LEDs for various link indications
- 1 fault indication LED controlled by the IPMI controller
- 1 general purpose LED controlled by the FPGA/CPU

Operating System Support
- OK-1, QNX, LINUX

Power Consumption
- 12 V, 2A max.

Environmental Conditions
- Operating temp.: 0°C to +55°C with forced cooling
- Storage temp.: -40°C to +85°C
- Relative humidity: 10% to 90% rh noncondensing

Standard Compliance
- PICMG AMC.0 Rev. 2.0
- PICMG AMC.1 Rev. 1.0
- PICMG AMC.2 Rev. 1.0 (Type E2)
- PCIe Base Spec. Rev. 1.1
- PICMG SFP.0 Rev. 1.0
- PICMG SFP.1 Rev. 1.0
- IPMI Specification v2.0 Rev. 1.0
- PICMG µTCA.0 Rev. 1.0