cPCI-Extender

PMC Module Extender

Reference Manual

Version 1.1

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Note:

The release of the Hardware Manual is related to a certain HW board revision given in the document title. For HW revisions earlier than the one given in the document title please contact N.A.T. for the corresponding older Hardware Manual release.

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1 Introduction

The cPCI-Extender is a passive cPCI extender board intended for use with cPCI boards for testing and debug purposes. It eases debugging of cPCI boards by enabling the user to access the module under test from both sides, install debug port cables, and allow access for measurement of all PCI and I/O signals from the module.

2 Technical Specifications

2.1 Bus Interface

- PCI bus 64 bit, 66 MHz and hot swap signals supported
- all J3 / J5 I/O signals routed
- H.110 implementation on J4

2.2 Test Equipment Access Points

The module is equipped with connector rows which are directly plug-compatible to Tectronix logic analyzers.

2.3 Power Supply

The cPCI-Extender draws very little power from the carrier supplies. Current drawn from +3.3V, +5V, +12V, -12V, V(I/O) is less than 10mA each.
+3.3V, +5V, V(I/O), and GND are connected to separate power planes.

All power supplies drive signalling LEDs. All power supplies may be cut by opening wire bridges for current measurements.

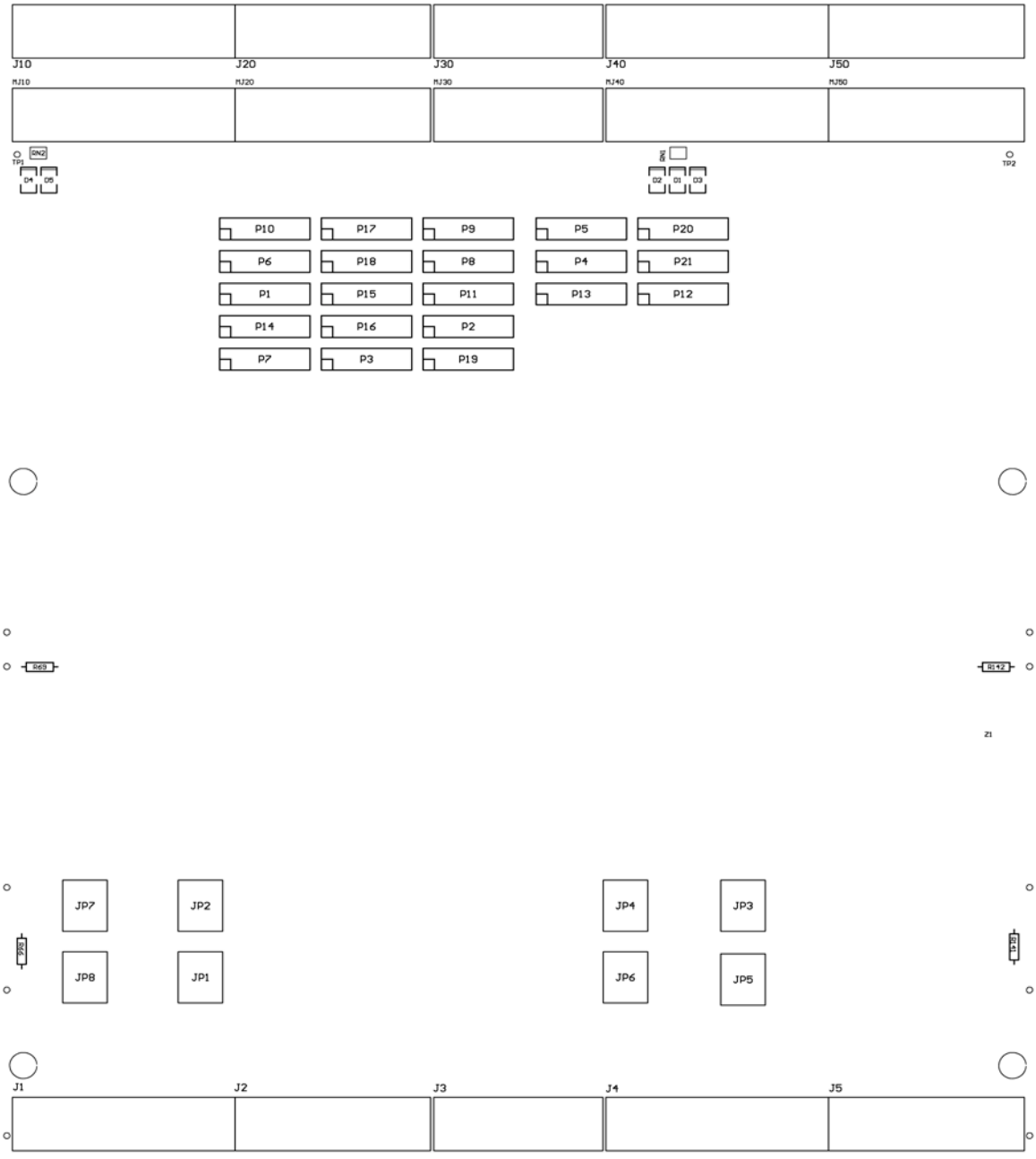
2.4 Environment

Temperature:	-40 – +85°C	operating and storage
Humidity:	5 – 90% rh	not condensing

3 Hardware Description

This chapter contains a brief description of the functional blocks of the cPCI-Extender extender board.

Figure 1



3.1 Hardware Overview

The cPCI-Extender is a passive extender board, i.e. it does not contain any circuitry apart from 2 cPCI connector sets (J1 – J5 plugging into the backplane, J10 – J50 for acceptance of the board under test).

Connectors MJ10 – MJ50 carry all PCI bus signals, I/O signals, and H.110 specific signals routed between the two sets of cPCI connectors for access by measuring equipment. These connectors are not assembled by default. Signals can be monitored by probing the connector holes.

The signals on P1 – P21 connectors are grouped by 8 and may be easily connected to a logic analyzer probe. One row of these double-row connectors carries the signals, the other is grounded. The male headers assembled fit directly into the probes of e.g. a Tectronix TLA logic analyzer series.

3.2 LEDs, Testpins, and Wire Bridges

There are 5 LEDs and 10 test pins assembled on the cPCI-Extender; two test pins / one LED for every power supply voltage, and two test pins for GND, suitable e.g. for the connection of GND cables of scope probes. The relationship between test points, LEDs, and wire bridges is shown below:

Table 1: LEDs and Testpoints

LED	Supply	Testpoint	Wire Bridge
	+5V_IN	JP5,1 + 2	JP5 / JP3
LED D1	+5V_OUT	JP3,1 + 2	both pins
	+3.3V_IN	JP6,1 + 2	JP6 / JP4
LED D2	+3.3V_OUT	JP4,1 + 2	both pins
	V(I/O)_IN	JP1,1 + 2	JP1 / JP2
LED D3	V(I/O)_OUT	JP2,1 + 2	both pins
	-12V_IN	JP7, 2	JP7 / JP8
LED D5	-12V_OUT	JP8, 2	pins 2
	+12V_IN	JP7, 1	JP7 / JP8
LED D4	+12V_OUT1	JP8, 1	pins 1
	GND	TP1	
	GND	TP2	

Opening the wire bridges connecting Vx_IN and Vx_OUT allows connection of an ampere meter between the respective test points for supply current measurement of every voltage.

4 Connectors

4.1 Compact PCI Backplane Connectors J1 / J10 / MJ10

Table 2: Compact PCI Backplane Connector J1 / J10 / MJ10 Rows A – C

Pin No.	Row A PCI-Signal	Row B PCI-Signal	Row C PCI-Signal
1	5V	-12V	/TRST
2	TCK	5V	TMS
3	/INTA	/INTB	/INTC
4	nc	/HEALTHY	V(I/O)
5	nc	nc	/RST
6	/REQ0*	GND	3.3V
7	AD30	AD29	AD28
8	AD26	GND	V(I/O)
9	/C/BE3	IDSEL	AD23
10	AD21	GND	3.3V
11	AD18	AD17	AD16
12	Key Area		
13			
14			
15	3.3V	/FRAME	/IRDY
16	/DEVSEL	GND	V(I/O)
17	3.3V	nc	nc
18	/SERR	GND	3.3V
19	3.3V	AD15	AD14
20	AD12	GND	V(I/O)
21	3.3V	AD9	AD8
22	AD7	GND	3.3V
23	3.3V	AD4	AD3
24	AD1	5V	V(I/O)
25	5V	/REQ64	/ENUM

* /REQ0 in system slot, /REQ in peripheral slot

Table 3: Compact PCI Backplane Connector J1 / J10 / MJ10 Rows D – F

Pin No.	Row D PCI-Signal	Row E PCI-Signal	Row F PCI-Signal
1	+12V	5V	GND
2	nc	TDI	GND
3	5V	/INTD	GND
4	INTP	INTS	GND
5	GND	/GNT0*	GND
6	CLK	AD31	GND
7	GND	AD27	GND
8	AD25	AD24	GND
9	GND	AD22	GND
10	AD20	AD19	GND
11	GND	/C/BE2	GND
12	Key Area		
13			
14			
15	/BD_SEL	/TRDY	GND
16	/STOP	/LOCK	GND
17	GND	/PERR	GND
18	PAR	/C/BE1	GND
19	GND	AD13	GND
20	AD11	AD10	GND
21	M66EN	/C/BE0	GND
22	AD6	AD5	GND
23	5V	AD2	GND
24	AD0	/ACK64	GND
25	3.3V	5V	GND

* /GNT0 in system slot, /GNT in peripheral slot

Connector descriptors J1 – J5 refer to cPCI connectors plugging into the backplane, connector descriptors J10 – J50 refer to cPCI connectors for acceptance of the board under test, connector descriptors MJ10 – MJ50 refer to measurement points for all PCI, H.110, and I/O signals.

4.2 Compact PCI Backplane Connector J2 / J20 / MJ20

Table 4: Compact PCI Backplane Connector J2 / J20 / MJ20 Rows A – C

Pin No.	Row A PCI-Signal	Row B PCI-Signal	Row C PCI-Signal
1	nc / CLK1**	GND	/REQ1*
2	nc / CLK2**	nc / CLK3**	/SYSEN
3	nc / CLK4**	GND	/GNT3*
4	V(I/O)	nc	/C/BE7
5	/C/BE5	GND	V(I/O)
6	AD63	AD62	AD61
7	AD59	GND	V(I/O)
8	AD56	AD55	AD54
9	AD52	GND	V(I/O)
10	AD49	AD48	AD47
11	AD45	GND	V(I/O)
12	AD42	AD41	AD40
13	AD38	GND	V(I/O)
14	AD35	AD34	AD33
15	nc	GND	/FAL
16	nc	nc	/DEG
17	nc	GND	/PRST
18	nc	GND	nc
19	GND	GND	nc
20	nc / CLK5**	GND	nc
21	nc / CLK6**	GND	nc
22	GA4	GA3	GA2

* driven only when located in system slot
** connected only when located in system slot, nc in peripheral slot

Table 5: Compact PCI Backplane Connector J2 / J20 / MJ20 Rows D – F

Pin No.	Row D PCI-Signal	Row E PCI-Signal	Row F PCI-Signal
1	/GNT1*	/REQ2*	GND
2	/GNT2*	/REQ3*	GND
3	/REQ4*	/GNT4*	GND
4	GND	/C/BE6	GND
5	/C/BE4	PAR64	GND
6	GND	AD60	GND
7	AD58	AD57	GND
8	GND	AD53	GND
9	AD51	AD50	GND
10	GND	AD46	GND
11	AD44	AD43	GND
12	GND	AD39	GND
13	AD37	AD36	GND
14	GND	AD32	GND
15	/REQ5*	/GNT5*	GND
16	GND	nc	GND
17	/REQ6*	/GNT6*	GND
18	GND	nc	GND
19	nc	nc	GND
20	GND	nc	GND
21	nc	nc	GND
22	GA1	GA0	GND

* driven only when located in system slot

4.3 Compact PCI Backplane Connector J3 / J30 / MJ30

Table 6: Compact PCI Backplane Connector J3 / J30 / MJ30 Rows A – C

Pin No.	Row A Signal	Row B Signal	Row C Signal
1	cPCI IO	cPCI IO	cPCI IO
2	cPCI IO	cPCI IO	cPCI IO
3	cPCI IO	cPCI IO	cPCI IO
4	cPCI IO	cPCI IO	cPCI IO
5	cPCI IO	cPCI IO	cPCI IO
6	cPCI IO	cPCI IO	cPCI IO
7	cPCI IO	cPCI IO	cPCI IO
8	cPCI IO	cPCI IO	cPCI IO
9	cPCI IO	cPCI IO	cPCI IO
10	cPCI IO	cPCI IO	cPCI IO
11	cPCI IO	cPCI IO	cPCI IO
12	cPCI IO	cPCI IO	cPCI IO
13	cPCI IO	cPCI IO	cPCI IO
14	cPCI IO	cPCI IO	cPCI IO
15	cPCI IO	cPCI IO	cPCI IO
16	cPCI IO	cPCI IO	cPCI IO
17	cPCI IO	cPCI IO	cPCI IO
18	cPCI IO	cPCI IO	cPCI IO
19	cPCI IO	cPCI IO	cPCI IO

Table 7: Compact PCI Backplane Connector J3 / J30 / MJ30 Rows D – F

Pin No.	Row D Signal	Row E Signal	Row F Signal
1	cPCI IO	cPCI IO	cPCI IO
2	cPCI IO	cPCI IO	cPCI IO
3	cPCI IO	cPCI IO	cPCI IO
4	cPCI IO	cPCI IO	cPCI IO
5	cPCI IO	cPCI IO	cPCI IO
6	cPCI IO	cPCI IO	cPCI IO
7	cPCI IO	cPCI IO	cPCI IO
8	cPCI IO	cPCI IO	cPCI IO
9	cPCI IO	cPCI IO	cPCI IO
10	cPCI IO	cPCI IO	cPCI IO
11	cPCI IO	cPCI IO	cPCI IO
12	cPCI IO	cPCI IO	cPCI IO
13	cPCI IO	cPCI IO	cPCI IO
14	cPCI IO	cPCI IO	cPCI IO
15	cPCI IO	cPCI IO	cPCI IO
16	cPCI IO	cPCI IO	cPCI IO
17	cPCI IO	cPCI IO	cPCI IO
18	cPCI IO	cPCI IO	cPCI IO
19	cPCI IO	cPCI IO	cPCI IO

All cPCI I/O signals are connected 1 : 1 between J3 / J30 / MJ30.

4.4 Compact PCI Backplane Connector J4 / J40 / MJ40

Compact PCI backplane connector J4 carries the H.110 bus signals.

Table 8: Compact PCI Backplane Connector J4 / J40 / MJ40 Rows A – C

Pin No.	Row A Signal	Row B Signal	Row C Signal
1	CT_D0	3.3V	CT_D1
2	CT_D4	CT_D5	CT_D6
3	CT_D8	CT_D9	CT_D10
4	CT_D11	5V	CT_D12
5	CT_D13	CT_D14	CT_D15
6	CT_D16	CT_D17	CT_D18
7	CT_D19	5V	CT_D20
8	CT_D21	CT_D22	CT_D23
9	CT_D24	CT_D25	CT_D26
10	CT_D27	3.3V	CT_D28
11	CT_D29	CT_D30	CT_D31
12	Key Area		
13			
14			
15	nc	nc	nc
16	nc	nc	nc
17	nc	nc	nc
18	nc	nc	nc
19	nc	nc	nc
20	nc	nc	nc
21	nc	nc	nc
22	nc	nc	nc
23	nc	nc	/CT_EN
24	GA4_J4	GA3_J4	GA2_J4
25	SGA4	SGA3	SGA2

Table 9: Compact PCI Backplane Connector J4 / J40 / MJ40 Rows D – F

Pin No.	Row D Signal	Row E Signal	Row F Signal
1	CT_D2	CT_D3	GND
2	CT_D7	GND	GND
3	GND	SCLKX2	GND
4	3.3V	SCLK	GND
5	3.3V	CT_NETREF2	GND
6	GND	CT_NETREF1	GND
7	GND	CT_C8B	GND
8	5V	CT_C8A	GND
9	GND	/FSYNC	GND
10	5V	CT_FRAMEB	GND
11	V(I/O)	CT_FRAMEA	GND
12	Key Area		
13			
14			
15	nc	nc	nc
16	nc	nc	nc
17	nc	nc	nc
18	nc	nc	nc
19	nc	nc	nc
20	nc	nc	nc
21	nc	nc	SGND*
22	nc	nc	SGND*
23	nc	nc	SGND*
24	GA1_J4	GA0_J4	SGND*
25	SGA1	SGA0	SGND*

** SGND is the protective GND of the board case and shielding, connected also to the front panel.

4.5 Compact PCI Backplane Connector J5 / J50 / MJ50

Table 10: Compact PCI Backplane Connector J5 / J50 / MJ50 Rows A – C

Pin No.	Row A Signal	Row B Signal	Row C Signal
1	cPCI IO	cPCI IO	cPCI IO
2	cPCI IO	cPCI IO	cPCI IO
3	cPCI IO	cPCI IO	cPCI IO
4	cPCI IO	cPCI IO	cPCI IO
5	cPCI IO	cPCI IO	cPCI IO
6	cPCI IO	cPCI IO	cPCI IO
7	cPCI IO	cPCI IO	cPCI IO
8	cPCI IO	cPCI IO	cPCI IO
9	cPCI IO	cPCI IO	cPCI IO
10	cPCI IO	cPCI IO	cPCI IO
11	cPCI IO	cPCI IO	cPCI IO
12	cPCI IO	cPCI IO	cPCI IO
13	cPCI IO	cPCI IO	cPCI IO
14	cPCI IO	cPCI IO	cPCI IO
15	cPCI IO	cPCI IO	cPCI IO
16	cPCI IO	cPCI IO	cPCI IO
17	cPCI IO	cPCI IO	cPCI IO
18	cPCI IO	cPCI IO	cPCI IO
19	cPCI IO	cPCI IO	cPCI IO
20	cPCI IO	cPCI IO	cPCI IO
21	cPCI IO	cPCI IO	cPCI IO
22	cPCI IO	cPCI IO	cPCI IO

Table 11: Compact PCI Backplane Connector J5 / J50 / MJ50 Rows D – F

Pin No.	Row D Signal	Row E Signal	Row F Signal
1	cPCI IO	cPCI IO	cPCI IO
2	cPCI IO	cPCI IO	cPCI IO
3	cPCI IO	cPCI IO	cPCI IO
4	cPCI IO	cPCI IO	cPCI IO
5	cPCI IO	cPCI IO	cPCI IO
6	cPCI IO	cPCI IO	cPCI IO
7	cPCI IO	cPCI IO	cPCI IO
8	cPCI IO	cPCI IO	cPCI IO
9	cPCI IO	cPCI IO	cPCI IO
10	cPCI IO	cPCI IO	cPCI IO
11	cPCI IO	cPCI IO	cPCI IO
12	cPCI IO	cPCI IO	cPCI IO
13	cPCI IO	cPCI IO	cPCI IO
14	cPCI IO	cPCI IO	cPCI IO
15	cPCI IO	cPCI IO	cPCI IO
16	cPCI IO	cPCI IO	cPCI IO
17	cPCI IO	cPCI IO	cPCI IO
18	cPCI IO	cPCI IO	cPCI IO
19	cPCI IO	cPCI IO	cPCI IO
20	cPCI IO	cPCI IO	cPCI IO
21	cPCI IO	cPCI IO	cPCI IO
22	cPCI IO	cPCI IO	cPCI IO

All cPCI I/O signals are connected 1 : 1 between J5 / J50 / MJ50.

4.6 Connectors for PCI and H.110 Signal Measurement

Connectors P1 – P21 carry all PCI bus and H.110 specific signals. These connectors are intended for use with measurement equipment. P1 – P21 are suitable for direct connection to logic analyzers, e.g. the Tectronix TLA logic analyzer series.

Table 12: Connector P1

Pin	Signal	Signal	Pin
1	GND	PCICLK	2
3	GND	FRAME#	4
5	GND	DEVSEL#	6
7	GND	IDSEL	8
9	GND	IRDY#	10
11	GND	TRDY#	12
13	GND	STOP#	14
15	GND	PCIRST#	16

Table 13: Connector P2

Pin	Signal	Signal	Pin
1	GND	PERR#	2
3	GND	SERR#	4
5	GND	REQ0#	6
7	GND	GNT0#	8
9	GND	REQ64#	10
11	GND	ACK64#	12
13	GND	PAR	14
15	GND	LOCK#	16

Table 14: Connector P3

Pin	Signal	Signal	Pin
1	GND	C/BE0#	2
3	GND	C/BE1#	4
5	GND	C/BE2#	6
7	GND	C/BE3#	8
9	GND	C/BE4#	10
11	GND	C/BE5#	12
13	GND	C/BE6#	14
15	GND	C/BE7#	16

Table 15: Connector P4

Pin	Signal	Signal	Pin
1	GND	CT_D0	2
3	GND	CT_D1	4
5	GND	CT_D2	6
7	GND	CT_D3	8
9	GND	CT_D4	10
11	GND	CT_D5	12
13	GND	CT_D6	14
15	GND	CT_D7	16

Table 16: Connector P5

Pin	Signal	Signal	Pin
1	GND	FSYNC#	2
3	GND	SCLKx2#	4
5	GND	SCLK	6
7	GND	nc	8
9	GND	nc	10
11	GND	nc	12
13	GND	PRST#	14
15	GND	PCIXCAP	16

Table 17: Connector P6

Pin	Signal	Signal	Pin
1	GND	PCI_AD31	2
3	GND	PCI_AD30	4
5	GND	PCI_AD29	6
7	GND	PCI_AD28	8
9	GND	PCI_AD27	10
11	GND	PCI_AD26	12
13	GND	PCI_AD25	14
15	GND	PCI_AD24	16

Table 18: Connector P7

Pin	Signal	Signal	Pin
1	GND	PCI_AD23	2
3	GND	PCI_AD22	4
5	GND	PCI_AD21	6
7	GND	PCI_AD20	8
9	GND	PCI_AD19	10
11	GND	PCI_AD18	12
13	GND	PCI_AD17	14
15	GND	PCI_AD16	16

Table 19: Connector P8

Pin	Signal	Signal	Pin
1	GND	PCI_AD63	2
3	GND	PCI_AD62	4
5	GND	PCI_AD61	6
7	GND	PCI_AD60	8
9	GND	PCI_AD59	10
11	GND	PCI_AD58	12
13	GND	PCI_AD57	14
15	GND	PCI_AD56	16

Table 20: Connector P9

Pin	Signal	Signal	Pin
1	GND	PCI_AD55	2
3	GND	PCI_AD54	4
5	GND	PCI_AD53	6
7	GND	PCI_AD52	8
9	GND	PCI_AD51	10
11	GND	PCI_AD50	12
13	GND	PCI_AD49	14
15	GND	PCI_AD48	16

Table 21: Connector P10

Pin	Signal	Signal	Pin
1	GND	INTA#	2
3	GND	INTB#	4
5	GND	INTC#	6
7	GND	INTD#	8
9	GND	INTS	10
11	GND	INTP	12
13	GND	FAL#	14
15	GND	DEG#	16

Table 22: Connector P11

Pin	Signal	Signal	Pin
1	GND	REQ1#	2
3	GND	REQ2#	4
5	GND	REQ3#	6
7	GND	REQ4#	8
9	GND	REQ5#	10
11	GND	REQ6#	12
13	GND	ENUM#	14
15	GND	HEALTHY#	16

Table 23: Connector P12

Pin	Signal	Signal	Pin
1	GND	CT_D8	2
3	GND	CT_D9	4
5	GND	CT_D10	6
7	GND	CT_D11	8
9	GND	CT_D12	10
11	GND	CT_D13	12
13	GND	CT_D14	14
15	GND	CT_D15	16

Table 24: Connector P13

Pin	Signal	Signal	Pin
1	GND	CT_D16	2
3	GND	CT_D17	4
5	GND	CT_D18	6
7	GND	CT_D19	8
9	GND	CT_D20	10
11	GND	CT_D21	12
13	GND	CT_D22	14
15	GND	CT_D23	16

Table 25: Connector P14

Pin	Signal	Signal	Pin
1	GND	PCI_AD15	2
3	GND	PCI_AD14	4
5	GND	PCI_AD13	6
7	GND	PCI_AD12	8
9	GND	PCI_AD11	10
11	GND	PCI_AD10	12
13	GND	PCI_AD9	14
15	GND	PCI_AD8	16

Table 26: Connector P15

Pin	Signal	Signal	Pin
1	GND	PCI_AD7	2
3	GND	PCI_AD6	4
5	GND	PCI_AD5	6
7	GND	PCI_AD4	8
9	GND	PCI_AD3	10
11	GND	PCI_AD3	12
13	GND	PCI_AD2	14
15	GND	PCI_AD0	16

Table 27: Connector P16

Pin	Signal	Signal	Pin
1	GND	PCI_AD47	2
3	GND	PCI_AD46	4
5	GND	PCI_AD45	6
7	GND	PCI_AD44	8
9	GND	PCI_AD43	10
11	GND	PCI_AD42	12
13	GND	PCI_AD41	14
15	GND	PCI_AD40	16

Table 28: Connector P17

Pin	Signal	Signal	Pin
1	GND	PCI_AD39	2
3	GND	PCI_AD38	4
5	GND	PCI_AD37	6
7	GND	PCI_AD36	8
9	GND	PCI_AD35	10
11	GND	PCI_AD34	12
13	GND	PCI_AD33	14
15	GND	PCI_AD32	16

Table 29: Connector P18

Pin	Signal	Signal	Pin
1	GND	GNT1#	2
3	GND	GNT2#	4
5	GND	GNT3#	6
7	GND	GNT4#	8
9	GND	GNT5#	10
11	GND	GNT6#	12
13	GND	PAR64	14
15	GND	SYSEN#	16

Table 30: Connector P19

Pin	Signal	Signal	Pin
1	GND	CLK1	2
3	GND	CLK2	4
5	GND	CLK3	6
7	GND	CLK4	8
9	GND	CLK5	10
11	GND	CLK6	12
13	GND	BD_SEL#	14
15	GND	M66EN	16

Table 31: Connector P20

Pin	Signal	Signal	Pin
1	GND	CT_D24	2
3	GND	CT_D25	4
5	GND	CT_D26	6
7	GND	CT_D27	8
9	GND	CT_D28	10
11	GND	CT_D29	12
13	GND	CT_D30	14
15	GND	CT_D31	16

Table 32: Connector P21

Pin	Signal	Signal	Pin
1	GND	CT_FRAME_B	2
3	GND	CT_C8_A	4
5	GND	CT_NETREF1	6
7	GND	CT_NETREF2	8
9	GND	nc	10
11	GND	nc	12
13	GND	CT_FRAME_A	14
15	GND	CT_C8_B	16

5 Document's History

Version	Date	Description	Author
1.0	4.2.2003	Initial Version	ga
1.1	16.12.2004	CT_FRAME_x mixup corrected	ga