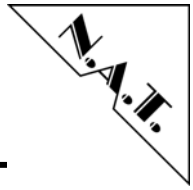

NPMC-8266-OC3
Telecom PMC Module
Technical Reference Manual V1.5

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Note:

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Conventions

If not otherwise specified, addresses and memory maps are written in hexadecimal notation, identified by *0x*.
Table 1 gives a list of the abbreviations used in this document:

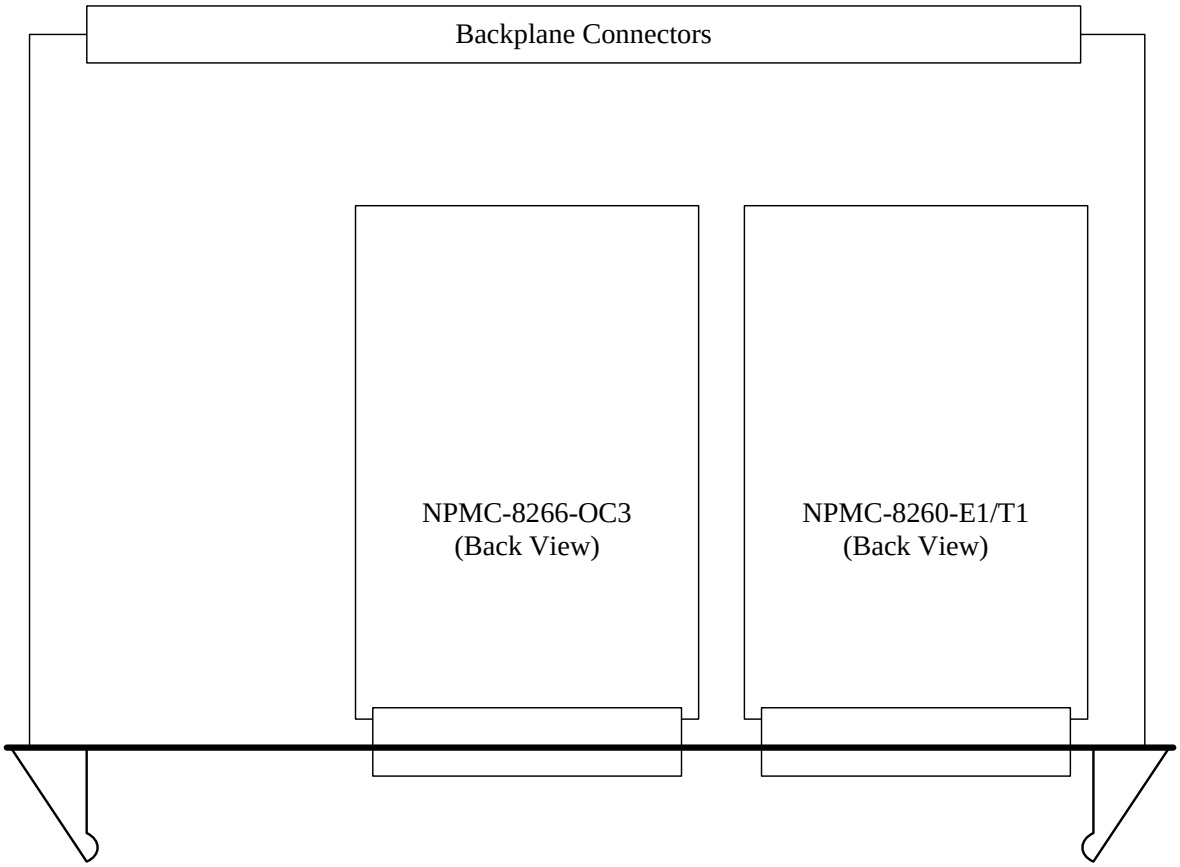
Table 1: List of used abbreviations

Abbreviation	Description
60x bus	PowerPC processor bus
b	Bit, binary
B	byte
CPU	Central Processing Unit
DMA	Direct Memory Access
E1	2.048 Mbit G.703 Interface
Flash	Programmable ROM
H.110	Time-Slot Interchange Bus
J1	1,544 Mbit G.703 Interface (Japan)
K	kilo (factor 400 in hex, factor 1024 in decimal)
LIU	Line Interface Unit
M	mega (factor 10,0000 in hex, factor 1,048,576 in decimal)
MHz	1,000,000 Herz
MPC8266	Embedded processors from Motorola
PowerQUICC II	MPC8266
RAM	Random Access Memory
ROM	Read Only Memory
SCbus	Time-Slot Interchange Bus of the SCSA, subset of H.110 bus
SCC	Serial Communication Controller of the MPC8266
SCSA	Signal Computing System Architecture
SDRAM	Synchronous Dynamic RAM
SMC	Serial Communication Controller of the MPC8266
SRAM	Static RAM
T1	1,544 Mbit G.703 Interface (USA)
TDM	Time Division Multiplex
TSI	Time Slot Interchange
TSA	Time Slot Assigner
UTOPIA II	bus interface for ATM PHY
ATM	asynchron transfer mode
PHY	physical layer device

1 Introduction

The **NPMC-8266-OC3** is a high performance standard CPU PCI Mezzanine Card Type 1. It can be plugged onto any carrier board supporting PMC standards:

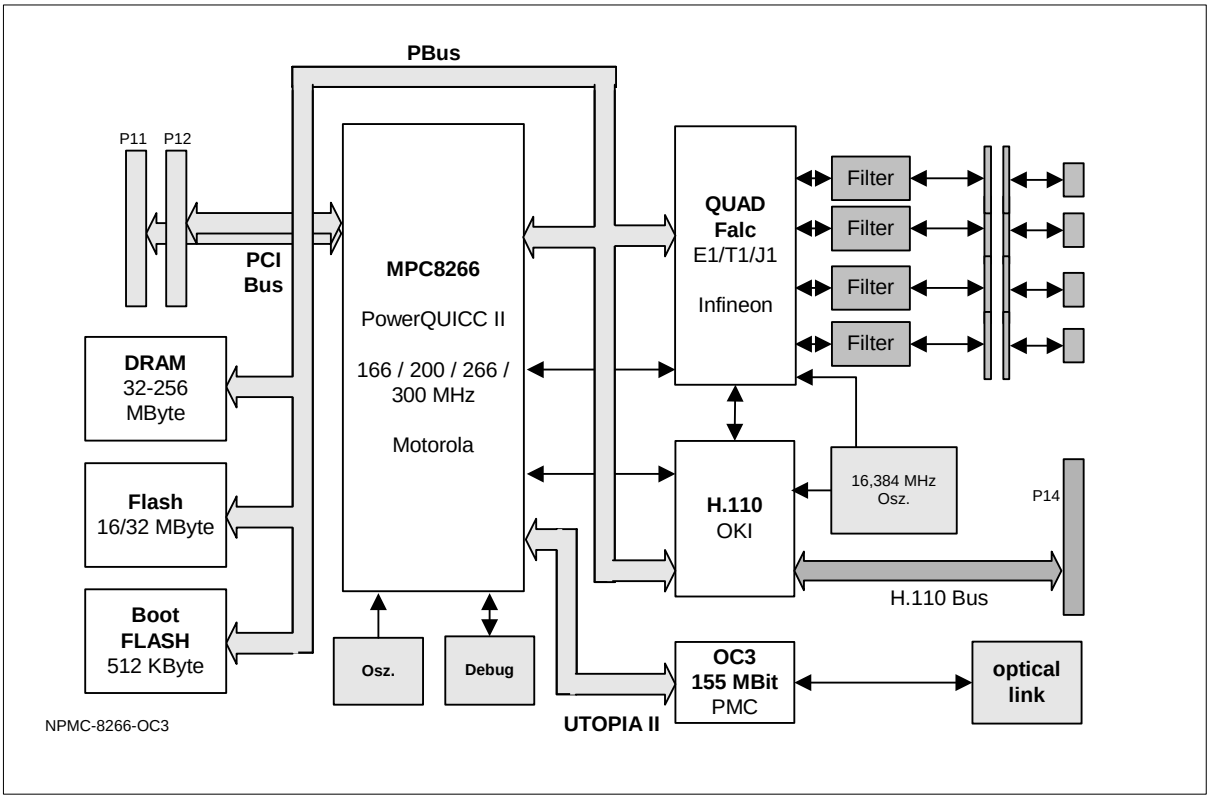
Figure 1: NPMC-8266-OC3 on a carrier board (VMEbus, cPCI)



The **NPMC-8266-OC3** has the following major features on-board:

- PowerQUICC II MPC8266 based Embedded PowerPC Architecture
- Front-panel I/O
- 32 bit / 66 MHz PCI Bus interface Rev. 2.2
- 4 x E1 / T1 / J1 primary rate line interface
- 155 MBit OC3 interface
- H.110 / SCSA TSI bus
- 32 – 256 MB main memory (SDRAM)
- 4 – 32 MB FLASH

Figure 2: NPMC-8266-OC3 Block Diagram



1.1 Board Features

- **CPU**

  Depending on the assembled CPU the PowerQUICC II runs with a core clock frequency of 166 - 308 MHz.

- **Memory**

  SDRAM: The **NPMC-8266-OC3** provides 32 to 256 MB SDRAM onboard. The SDRAM is installed as a SODIMM SDRAM module. PC100-type modules of 32 MB, 64 MB, 128 MB, and 256 MB are supported. The SDRAM is 64 bit wide.

  Default: 32 MB installed

  Flash PROM: The 16-bit wide Flash PROM provides a capacity of 4 - 32 MB (assembly option).

  Default: 16 MB installed

- **Interfaces**

  PCI: The **NPMC-8266-OC3** includes a 32 bit 33/66 MHz PCI bus interface. This is implemented in the MPC8266 CPU.

  H.110: The **NPMC-8266-OC3** implements a 32 bit H.110 interface, which includes an SCbus interface on I/O-connector P14 according to PMC specifications. This is implemented by an OKI ML53812-2 TSI device.

- **I/O**

  E1/T1/J1: The module carries a PEB22554 (QuadFALC) framer, which implements four E1/T1/J1 interfaces.

  OC3: The MPC8266 CPU integrates a UTOPIA II interface. This is connected to an ATM/OC3 PHY, which connects to an optical link at the module's front panel. The PHY used is a PM5382 (S/UNI 1x155MBit).

  RS232: There is an RS232 interface available on the **NPMC-8266-OC3**, which is connected to the SMC1 interface of the MPC8266 CPU. This debug interface shares a connector with the BDM / JTAG interface.

  Note: The 4 E1/T1/J1 line interfaces and the OC3 optical link are connected to front panel connectors. The H.110/SCbus is connected to the PCI I/O connector.

1.2 Board Specification

Table 2: NPMC-8266-OC3 Features

Processor	PowerQUICC II MPC8266 based Embedded PowerPC Architecture, 166 to 308 MHz	
PMC-Module	Standard PCI Mezzanine Card Type 1, 3.3V signalling	
Front-I/O	2 RJ45 connectors, 1 SC/LC duplex optical transceiver	
Main Memory	32 - 256 MByte SDRAM PC100-type	
Flash PROM	4 – 32 MByte Flash PROM. On board programmable	
Firmware	OK1, VxWorks BSP (on request)	
Power consumption	3.3V 0.6A typ. 5.0V 0.3A typ.	
Environmental conditions	Temperature (operating):	0°C to +60°C with forced cooling
	Temperature (storage):	-40°C to +85°C
	Humidity:	10 % to 90 % rh noncondensing
Standards compliance	PCI Rev. 2.2 P1386.1 / Draft 2.4a	

2 Installation

2.1 Safety Note

To ensure proper functioning of the **NPMC-8266-OC3** during its usual life-time take the following precautions before handling the board.

CAUTION

Electrostatic discharge and incorrect board installation and uninstallation can damage circuits or shorten their lifetime.

- Before installing or uninstalling the **NPMC-8266-OC3** read this installation section
- Before installing or uninstalling the **NPMC-8266-OC3**, read the Installation Guide and the User's Manual of the carrier board used
- Before installing or uninstalling the **NPMC-8266-OC3** on a carrier board or both in a rack:
  - Check all installed boards and modules for steps that you have to take before turning on or off the power.
  - Take those steps.
  - Finally turn on or off the power.
- Before touching integrated circuits ensure to take all require precautions for handling electrostatic devices.
- Ensure that the **NPMC-8266-OC3** is connected to the carrier board via all PMC connectors and that the power is available on both PMC connectors (GND, +5V, and +3.3V).
- When operating the board in areas of strong electromagnetic radiation ensure that the module
  - is bolted the front panel or rack
  - and shielded by closed housing

CAUTION !!!

- The PCI interface supports **only** 3.3V signalling and is **NOT** 5V tolerant! Please install only on carrier boards which use 3.3V signalling voltage.

2.2 Installation Prerequisites and Requirements

IMPORTANT

Before powering up

- check this section for installation prerequisites and requirements

2.2.1 Requirements

The installation requires only

- a carrier board for connecting the **NPMC-8266-OC3**
- power supply

2.2.2 Power supply

The power supply for the **NPMC-8266-OC3** must meet the following specifications:

- required for the module:
  - +3.3V / 0.6A typical
  - +5.0V / 0.3A typical

2.2.3 Automatic Power Up

In the following situations the **NPMC-8266-OC3** will automatically be reset and proceed with a normal power up.

Voltage sensors

The voltage sensor generates a reset

- when +5V voltage level drops below 4,4V *
- when +5V voltage level rises above 5,6V *
- when +3.3V voltage level drops below 2,65V *
- when +3.3V voltage level rises above 3,9V *
- or when the carrier board signals a PCI Reset

Watchdog (if enabled)

* defined by: “PCI Specification Revision 2.2, Section 4.2.1.1 and Section 4.3.2”

2.3 Statement on Environmental Protection

2.3.1 Compliance to RoHS Directive

Directive 2002/95/EC of the European Comission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) predicts that all electrical and electronic equipment being put on the European market after June 30th, 2006 must contain lead, mercury, hexavalent chromium, polybrominated biphenyls (PBB) and polybrominated diphenyl ethers (PBDE) and cadmium in maximum concentration values of 0.1% respective 0.01% by weight in homogenous materials only.

As these harzadous substances are currently used with semiconductors, plastics (i.e. semiconductor packages, connectors) and soldering tin any hardware product is affected by the RoHS directive if it does not belong to one of the groups of products exempted from the RoHS directive.

Although many of hardware products of N.A.T. are exempted from the RoHS directive it is a declared policy of N.A.T. to provide all products fully compliant to the RoHS directive as soon as possible. For this purpose since January 31st, 2005 N.A.T. is requesting RoHS compliant deliveries from its suppliers. Special attention and care has been payed to the production cycle, so that whereever and whenever possible RoHS components are used with N.A.T. hardware products already.

2.3.2 Compliance to WEEE Directive

Directive 2002/95/EC of the European Comission on "Waste Electrical and Electronic Equipment" (WEEE) predicts that every manufacturer of electrical and electronical equipment which is put on the European market has to contribute to the reuse, recycling and other forms of recovery of such waste so as to reduce disposal. Moreover this directive refers to the Directive 2002/95/EC of the European Comission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS).

Having its main focus on private persons and households using such electrical and electronic equipment the directive also affects business-to-business relationships. The directive is quite restrictive on how such waste of private persons and households has to be handled by the supplier/manufacturer, however, it allows a greater flexibility in business-to-business relationships. This pays tribute to the fact with industrial use electrical and electronical products are commonly intergrated into larger and more complex envionments or systems that cannot easily be split up again when it comes to their disposal at the end of their life cycles.

As N.A.T. products are solely sold to industrial customers, by special arrangement at time of purchase the customer agreed to take the responsibility for a WEEE compliant disposal of the used N.A.T. product. Moreover, all N.A.T. products are marked according to the directive with a crossed out bin to indicate that these products within the European Community must not be disposed with regular waste.

If you have any questions on the policy of N.A.T. regarding the Directive 2002/95/EC of the European Comission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) or the Directive 2002/95/EC of the European Comission on "Waste Electrical and Electronic Equipment" (WEEE) please contact N.A.T. by phone or e-mail.

2.3.3 Compliance to CE Directive

Compliance to the CE directive is declared. A ‘CE’ sign can ce found on the PCB.

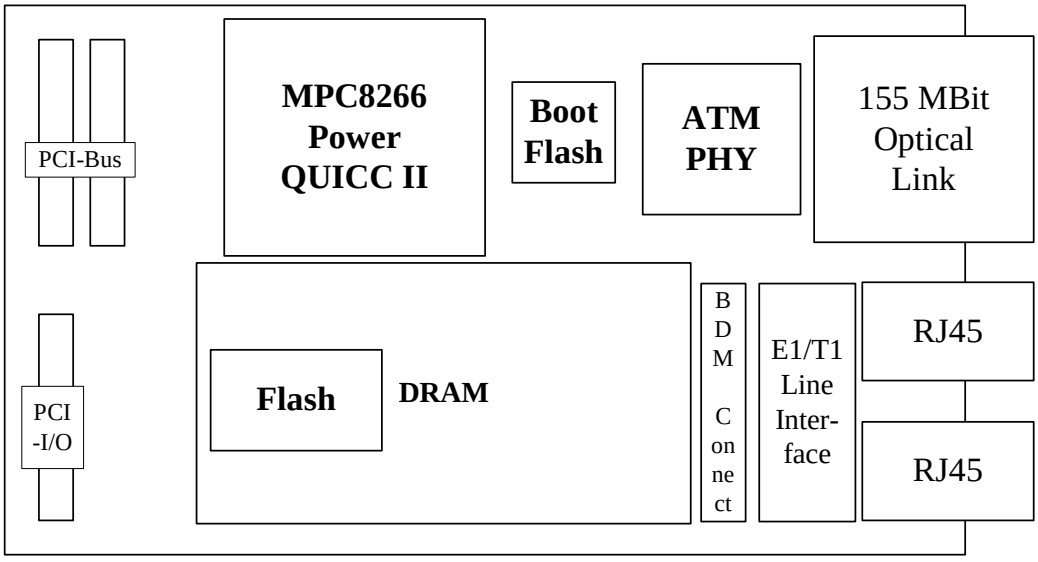
2.3.4 Product Safety

The board complies to EN60950 and UL1950.

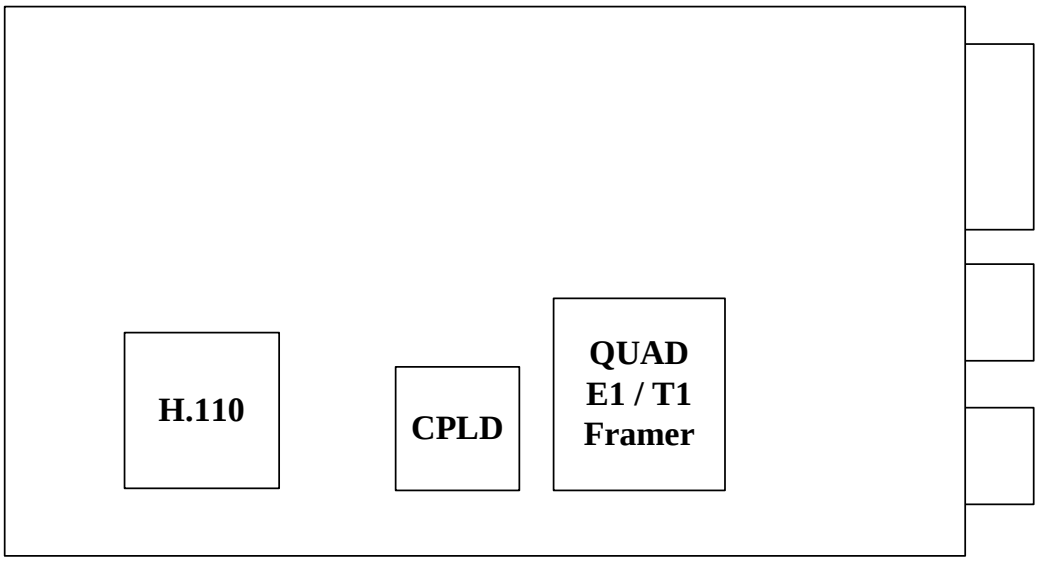
3 Location Overview

The figure 3 "Location diagram of the **NPMC-8266-OC3**" highlights the position of the important components. Depending on the board type it might be that the board does not include all components named in the location diagram.

Figure 3: Location diagram of the NPMC-8266-OC3



Top View



Bottom View

4 Functional Blocks

The **NPMC-8266-OC3** can be divided into a number of functional blocks, which are described in the following paragraphs.

4.1 Processor

The MPC8266 PowerQUICC II™ is a versatile communications processor that integrates on one chip a high-performance PowerPC™ RISC microprocessor, a very flexible system integration unit, and many communications peripheral controllers that can be used in a variety of applications, particularly in communications and networking systems.

The core is an embedded variant of the PowerPC MPC603e™ microprocessor with 16 Kbytes of instruction cache and 16 Kbytes of data cache and no floating-point unit (FPU). The system interface unit (SIU) consists of a flexible memory controller that interfaces to almost any user-defined memory system, and many other peripherals making this device a complete system on a chip.

The communications processor module (CPM) includes four serial communications controllers (SCCs) , with the addition of three high-performance communication channels that support new emerging protocols (for example, 155 Mbps ATM and Fast Ethernet). The MPC8266 has dedicated hardware that can handle up to 256 full-duplex, time-division-multiplexed logical channels, as well as DMA functionality executing memory to memory and memory to I/O transfers.

4.2 PCI Interface

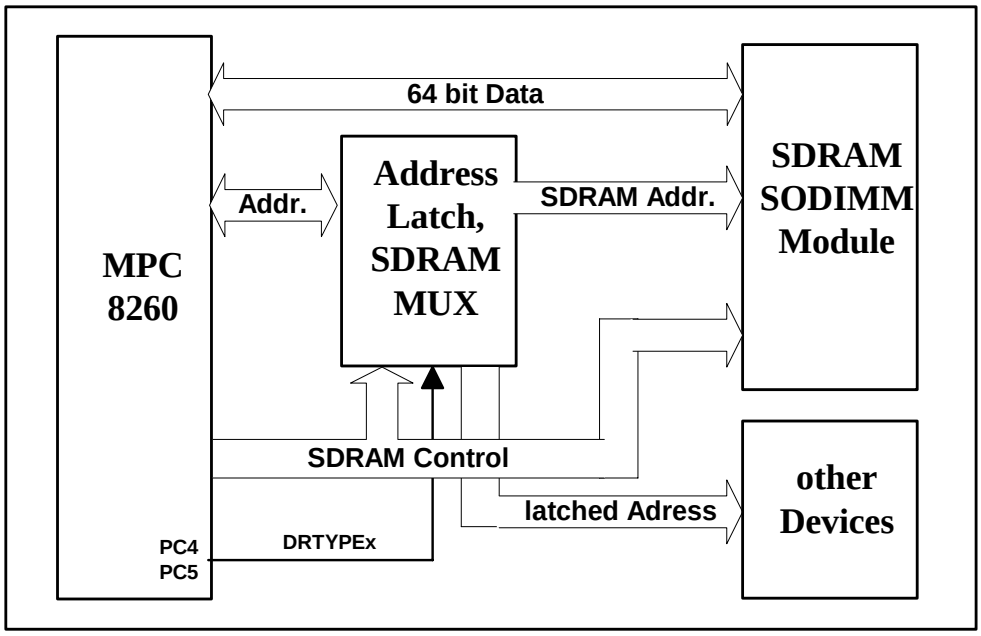
The MPC8266 integrates a 32 bit, 33/66 MHz PCI interface.

4.3 Memory

4.3.1 SDRAM

As the onboard SDRAM memory has to be accessed not only be the CPU, but also by the host through the PowerSpan PCI bridge, external address latches and multiplexers had to be implemented. The structure is shown in Figure 4 below.

Figure 4: Address / Data Paths to onboard Devices



The SDRAM is connected to the 60x bus interface of the MPC8266. The multiplexer organisation can be adjusted to different SDRAM types by the DRTYPEx selection signals. Suitable SDRAM modules must be of PC100 or PC133 type. Refer to **Chapter 4, Table 8 and 9** for further information on SODIMM modules.

4.3.2 FLASH

There are 2 FLASH devices implemented on the **NPMC-8266-OC3**, the main FLASH containing application software, and a Fallback FLASH containing a simple boot image with a small debug kernel. Which FLASH is the boot FLASH is decided by decoding of jumper JP4. If JP4 is installed, the Fallback FLASH is the boot device. If JP4 is not installed, the main FLASH is the boot device.

4.3.2.1 Main FLASH Memory

The main FLASH memory is connected to the upper 16 data bits D0 – 15 and to the latched address lines. The FLASH on the NPMC-8266-OC3 can be programmed either by the CPU (by appropriate software or through the BDM port) or by a PCI bus master. In the latter case the PowerQUICC II has to be prevented from booting from this FLASH while it does not contain a defined boot program, in order not to enter unknown states. This can be achieved by installing a jumper (JP3), which disables the MPC8266 CPU core after the following Power-Up cycle. This feature is used for programming the FLASH memory via the PCI bus. If JP3 is installed the Hardware Configuration Words for the CPU is loaded from an onboard CPLD. If JP3 is not installed, the Hardware Configuration Word is loaded from the first 256 bytes of the FLASH. Once the FLASH has been programmed, it may be reprogrammed without having to install JP3. Programming software is available on request. Please refer to section 5.4 for details on jumper JP3.

4.3.2.2 Fallback FLASH Memory

The Fallback FLASH memory is connected to the upper 8 data bits D0 – 7 and to the latched address lines. It is handled like the main FLASH described above.

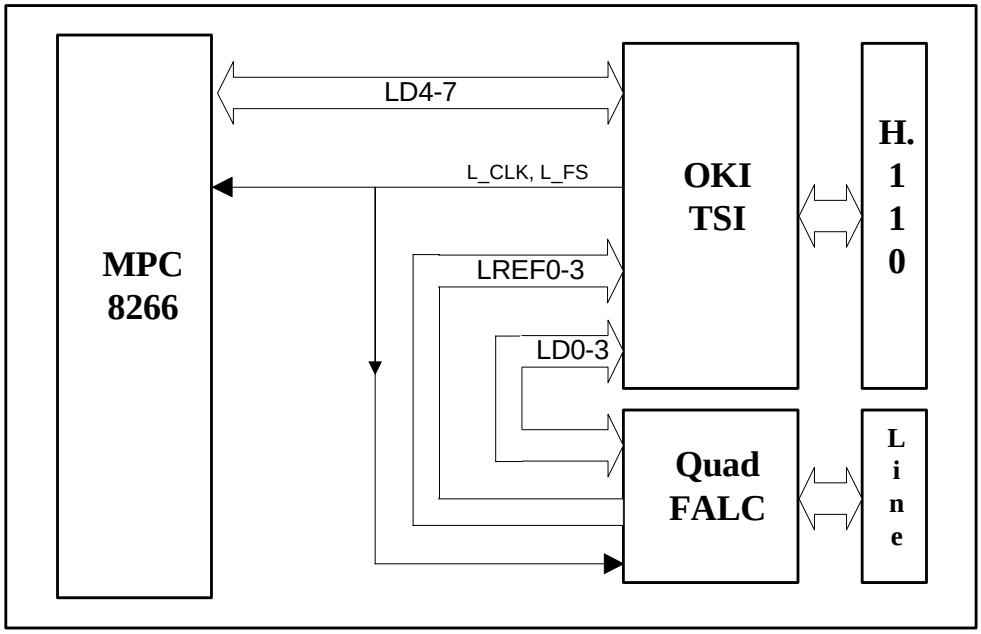
4.3.3 I^2C Devices

There are two I^2C devices on the NPMC-8266-OC3, which are connected to MPC8266 port pins; an EEPROM used for storage of board-specific information, and the EEPROM on the SODIMM SDRAM module, which contains vital data about the SDRAM module size and address organisation. This information is necessary, in order to be able to program the SDRAM controller functions appropriately. The SODIMM I^2C device defaults to a 24C02 type, the onboard EEPROM is a 24C08 device. The address of the EEPROM on the SDRAM SODIMM module is 0x0, the address of the other EEPROM is 0x4.

4.4 H.110 Bus Controller and Line Interfaces

4.4.1 Block Diagramm of the TDM Structure

Figure 5: Local TDM Bus Organisation and Synchronisation



4.4.2 Description of the TDM Structure

The TDM data are routed through the ML53812-2 TSI device. Hence, any timeslot switching between H.110 bus, framers, and CPU is possible. The TSI device derives its time base from one of the LREF signals coming from the framers, or from the H.110 bus. From this input it generates local clock and frame sync for the framers and the CPU to synchronize to. Timing reference for offboard routing devices can be provided by programming one of the local LREF signals to be output on one of the NETREFx signals. For detailed information please refer to the Motorola MPC8266, OKI ML53812-2, and Infineon PEB22554 User's Manuals.

4.4.3 SCbus Compatibility

The SCbus implemented on the NPMC-8266-OC3 is a sub-set of the H.110 bus. SCbus data lines correspond to H.110 data lines CT_D0 – 15. See chapter 5.8 (PMC P14 Connector) for reference. As an assembly option either the H.110 reference signal NETREF1 or NETREF2 may be connected to the corresponding SCbus signal SREF_8K.
By default, NETREF1 is connected to SREF_8K.

4.4.4 E1/T1/J1 Line Interfaces

The four E1/T1/J1 interfaces connect the Infineon QuadFLC framer to the front panel RJ45 connectors. Timing and interface characteristics can be set up by software within the QuadFALC, the correct line impedance is selected by programming the IMPSELA and IMPSELB port signals as described below in chapter 4. The line interfaces conform to EN60950 and G.703.

4.5 ATM Interface, OC3 Optical Link

The PM5382 ATM PHY is connected to the MPC8266 through the UTOPIA II interface. It connects to the front panel through an optical SC duplex transceiver (S3).

5 Hardware

5.1 Memory Map

All addresses are set up by programming the corresponding Chip-Select Decoder of the PowerQUICC II.

Table 3: Memory Map

Device	CS Line	Address	Function	Notes
main FLASH	CS0	programmable	Boot, user code	4/8/16/32 MByte Flash-Prom (16 bit wide)
fallback FLASH	CS1	programmable	Boot, user code	512 KByte FLASH-Prom (8 bit wide)
SDRAM	CS2	programmable	main memory, CS2 and CS3 share the same SODIMM	32 - 256 MByte SDRAM (64 bit wide)
SDRAM	CS3	programmable		
not used	CS4	not used		
ML53812	CS5	programmable	H.110 TSI	8 bit wide
PEB22554	CS6	programmable	QuadFALC	8 bit wide
PM5382	CS7	programmable	ATM PHY	8 bit wide
not used	CS8	not used		
not used	CS9	not used		
not used	CS10	not used		
not used	CS11	not used		

5.2 Definition of PowerQUICC II Port Pins

PowerQUICC II port pins are used to communicate with the framers and to set up some board configuration. In detail:

Table 4: PowerQUICC II Port Pin Usage (Port A)

Signal Function	PowerQUICC II Port A Pin	Description
UTOPIA TX ENB	PA31	UTOPIA Interface
UTOPIA TX CLAV	PA30	UTOPIA Interface
UTOPIA TX SOC	PA29	UTOPIA Interface
UTOPIA RX ENB	PA28	UTOPIA Interface
UTOPIA RX SOC	PA27	UTOPIA Interface
UTOPIA RX CLAV	PA26	UTOPIA Interface
UTOPIA TX D8	PA25	UTOPIA Interface
UTOPIA TX D9	PA24	UTOPIA Interface
UTOPIA TX D10	PA23	UTOPIA Interface
UTOPIA TX D11	PA22	UTOPIA Interface
UTOPIA TX D12	PA21	UTOPIA Interface
UTOPIA TX D13	PA20	UTOPIA Interface
UTOPIA TX D14	PA19	UTOPIA Interface
UTOPIA TX D15	PA18	UTOPIA Interface
UTOPIA RX D15	PA17	UTOPIA Interface
UTOPIA RX D14	PA16	UTOPIA Interface
UTOPIA RX D13	PA15	UTOPIA Interface
UTOPIA RX D12	PA14	UTOPIA Interface
UTOPIA RX D11	PA13	UTOPIA Interface
UTOPIA RX D10	PA12	UTOPIA Interface
UTOPIA RX D9	PA11	UTOPIA Interface
UTOPIA RX D8	PA10	UTOPIA Interface
TSI LDI4	PA9	Time Slot Assigner Bus data bit 4, output of the MPC8266, input to the ML53812 H.110 controller (Time Slot Interchange (TSI))
TSI LDO4	PA8	Time Slot Assigner Bus data bit 4, input to the MPC8266, output of the ML53812 H.110 controller (Time Slot Interchange (TSI))
TSI L_FS	PA7	Time Slot Assigner frame sync, input to the MPC8266, output of the ML53812 H.110 controller
TSI L_FS	PA6	TSA frame sync
SL4	PA5	SCbus geographical address
SL3	PA4	SCbus geographical address

TSI L_CLK1	PA3	Time Slot Assigner alternate clock, input to the MPC8266, output of the ML53812 H.110 controller
TSI L_CLK1	PA2	TSA alternate clock
SL2	PA1	SCbus geographical address
SL1	PA0	SCbus geographical address

Table 5: PowerQUICC II Port Pin Usage (Port B)

Signal Function	PowerQUICC II Port B Pin	Description
TSI LDI5	PB31	TSA data bus bit 5, TSI in
TSI LDO5	PB30	TSA data bus bit 5, TSI out
TSI L_FS1	PB29	TSA alternate frame sync
TSI L_FS1	PB28	TSA alternate frame sync
TSI LDI6	PB27	TSA data bus bit 6, TSI in
TSI LDO6	PB26	TSA data bus bit 6, TSI out
TSI L_FS1	PB25	TSA alternate frame sync
TSI L_FS1	PB24	TSA alternate frame sync
TSI LDI7	PB23	TSA data bus bit 7, TSI in
TSI LDO7	PB22	TSA data bus bit 7, TSI out
TSI L_FS1	PB21	TSA alternate frame sync
TSI L_FS1	PB20	TSA alternate frame sync
IMPSELA*	PB19	E1 line impedance select
IMPSELB*	PB18	E1 line impedance select
TSI L_CLK1	PB17	TSA alternate clock
TSI L_CLK1	PB16	TSA alternate clock
TSI LDI6	PB15	TSA data bus bit 6, TSI in
TSI LDO6	PB14	TSA data bus bit 6, TSI out
TSI L_FS	PB13	TSA frame sync
TSI L_FS	PB12	TSA frame sync
TSI LDI7	PB11	TSA data bus bit 7, TSI in
TSI LDO7	PB10	TSA data bus bit 7, TSI out
TSI L_FS	PB9	TSA frame sync
TSI L_FS	PB8	TSA frame sync
TSI LDI4	PB7	TSA data bus bit 4, TSI in
TSI LDO4	PB6	TSA data bus bit 4, TSI out
TSI L_FS1	PB5	TSA alternate frame sync
TSI L_FS1	PB4	TSA alternate frame sync

Table 6: PowerQUICC II Port Pin Usage (Port C)

Signal Function	PowerQUICC II Port C Pin	Description
TSI L_CLK	PC31	Time Slot Assigner clock, input to the MPC8266, output of the ML53812 H.110 controller
TSI L_CLK	PC30	TSA clock
TSI L_CLK	PC29	TSA clock
TSI L_CLK	PC28	TSA clock
TSI L_CLK	PC27	TSA clock
TSI L_CLK	PC26	TSA clock
TSI L_CLK	PC25	TSA clock
TSI L_CLK	PC24	TSA clock
LED4	PC23	Front Panel LED
LED3	PC22	Front Panel LED
LED2	PC21	Front Panel LED
LED1	PC20	Front Panel LED
TSI L_CLK1	PC19	Time Slot Assigner alternate clock, input to the MPC8266, output of the ML53812 H.110 controller
TSI L_CLK1	PC18	TSA alternate clock
TSI L_CLK1	PC17	TSA alternate clock
TSI L_CLK1	PC16	TSA alternate clock
UTOPIA TX ADDR0	PC15	UTOPIA Interface
UTOPIA RX ADDR0	PC14	UTOPIA Interface
UTOPIA TX ADDR1	PC13	UTOPIA Interface
UTOPIA RX ADDR1	PC12	UTOPIA Interface
SL0	PC11	SCbus geographical address
UTOPIA TX D2	PC10	UTOPIA Interface
UTOPIA TX D1	PC9	UTOPIA Interface
UTOPIA TX D0	PC8	UTOPIA Interface
UTOPIA TX ADDR2	PC7	UTOPIA Interface
UTOPIA RX ADDR2	PC6	UTOPIA Interface
DRTYPE0*	PC5	SDRAM control function
DRTYPE1*	PC4	SDRAM control function
FS0*	PC3	Framer PLL Select Signal
nc	PC2	not used
nc	PC1	not used
UTOPIA TX CLK	PC0	UTOPIA Interface

Signals with asterisk (*) are described in detail below.

Table 7: PowerQUICC II Port Pin Usage (Port D)

Signal Function	PowerQUICC II Port D Pin	Description
SDA_PQ*	PD31	I^2C Bus, data
SCL_PQ*	PD30	I^2C Bus, clock
UTOPIA RX ADDR3	PD29	UTOPIA Interface
UTOPIA TX D7	PD28	UTOPIA Interface
UTOPIA RX D7	PD27	UTOPIA Interface
UTOPIA RX D6	PD26	UTOPIA Interface
UTOPIA TX D6	PD25	UTOPIA Interface
UTOPIA RX D5	PD24	UTOPIA Interface
UTOPIA RX D4	PD23	UTOPIA Interface
UTOPIA TX D5	PD22	UTOPIA Interface
UTOPIA RX D3	PD21	UTOPIA Interface
UTOPIA RX D2	PD20	UTOPIA Interface
UTOPIA TX ADDR4	PD19	UTOPIA Interface
UTOPIA RX ADDR4	PD18	UTOPIA Interface
UTOPIA RX PRTY	PD17	UTOPIA Interface
UTOPIA TX PRTY	PD16	UTOPIA Interface
UTOPIA RX D1	PD15	UTOPIA Interface
UTOPIA RX D0	PD14	UTOPIA Interface
TSI LDI5	PD13	TSA data bus bit 7, TSI in
TSI LDO5	PD12	TSA data bus bit 7, TSI out
TSI L_FS	PD11	TSA frame sync
TSI L_FS	PD10	TSA frame sync
TXD1_SMC*	PD9	transmit data lines of the RS232 interface, SMC1
RXD1_SMC*	PD8	receive data lines of the RS232 interface, SMC1
UTOPIA TX ADDR3	PD7	UTOPIA Interface
UTOPIA TX D4	PD6	UTOPIA Interface
UTOPIA TX D3	PD5	UTOPIA Interface
UTOPIA RX CLK	PD4	UTOPIA Interface

Signals with asterisk (*) are described in detail below.

5.2.1 Signal Description

5.2.1.1 Selecting the ISDN Line Impedance

IMPSELA, IMPSELB — Line impedance select lines used for selection of 100 Ω (T1/J1), 120 Ω (E1), or 75 Ω (E1) receiver line termination

IMPSELA	IMPSELB	receiver line termination
0	0	100 Ω (T1/J1)
0	1	75 Ω (E1)
1	0	120 Ω (E1)
1	1	no termination selected (***default***)

5.2.1.2 Serial Line Interface Pins

RXD1_SMC, TXD1_SMC — receive data line of the RS232 interface, SMC1 on PD8; transmit data line of the RS232 interface, SMC1 on PD9

5.2.1.3 I^2C Interface Pins

SDA_PQ, SCL_PQ — I^2C interface connected to the SDRAM SODIMM EEPROM (address 0x0) and to the general purpose EEPROM U10 (24C08, address 0x4)

5.2.1.4 QuadFALC PLL Configuration Pins

FS0 — PLL function select signal, defines the clock driven to the QuadFALC framer chip. FS3 – FS1 are grounded at the PLL device.
The state of FS0 sets the input frequency of the analogue framer circuitry to be 1.544 MHz (FS0 = 0) or 2.048 MHz (FS0 = 1).

5.2.1.5 SDRAM Configuration Pins

DRTYPE0, DRTYPE1

Port pins used to set the correct multiplexing logic within Lattice U13. These pins code the size and array information of the SDRAM module installed. The correct binary value for DRTYPE1-0 has to be determined by reading the SDRAM SODIMM EEPROM contents. This EEPROM contains also further information needed to program the SDRAM controller of the MPC8266 appropriately, e.g. row start address and clock cycles needed for SDRAM access.
DRTYPEx settings refer to following SODIMM organisation:

Table 8: Supported SDRAM SODIMM Module Types

DRTYPE1 (PC4)	DRTYPE0 (PC5)	highest column address to be multiplexed	no. of SDRAM column addresses
0	0	SDA7	8
0	1	SDA8	9
1	0	SDA9	10
1	1	SDA11	11

SDAx refers to SDRAM SODIMM address pin.

Addresses to be programmed to be output on PowerQUICC II signals BNKSELx:

Table 9: BNKSELx Programming

DRTYPE1 (PC4)	DRTYPE0 (PC5)	BNKSEL2	BNKSEL1
0	0	PB_A19	PB_A20
0	1	PB_A18	PB_A19
1	0	PB_A17	PB_A18
1	1	PB_A16	PB_A17

PB_Ax refers to PowerQUICC II address line Ax. BNKSEL0 is not used.

Refer to chapter 7 of this manual and to the MPC8266 User's Manual for a detailed description of how to program the Memory Controller of the MPC8266.

5.3 CPU - PLL-Setup

The basic setting of the clocks is done by pulling the MODCK pins during /CPURST. /CPURST is the Reset input of the CPU and valid with Power-On RESET and /PCIRST. These are programmable through CPLD U25 (BA0-2). There are 5 additional pins (PCIMODCKx) responsible for setting the PLLs, which are also read during /PORESET. E.g. the default PLL setting for a MPC8266 CPU is MODCK1 - 3 = 100b and PMODCKH0 - 3 = 0111b for a 300/200 MHz CPU/CPM version.

5.4 Interrupt Structure

The **NPMC-8266-OC3** has the following Interrupt structure:

Table 10: Interrupt Structure

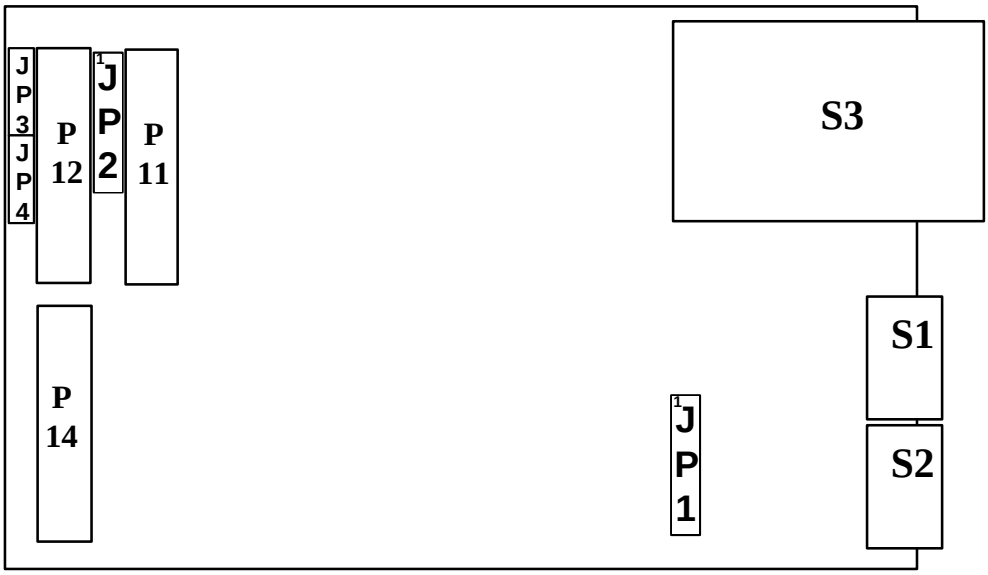
Interrupt source	PowerQUICC Interrupt level
NC	IRQ-Level 0 (highest level)
PM5382	IRQ-Level 1
ML53812	IRQ-Level 2
PEB22554	IRQ-Level 3
NC	IRQ-Level 4
NC	IRQ-Level 5
NC	IRQ-Level 6
NC	IRQ-Level 7 (lowest level)

Interrupts described as NC should be masked in the MPC8266 mask register.

6 Connectors

6.1 Connector Overview

Figure 6: Connectors of the NPMC-8266-OC3



Please refer to the following tables to look up the pin assignment of the NPMC-8266-OC3.

6.2 Connector JP1: BDM and JTAG connector

Table 11: Development Port / BDM and IEEE 1149.1 Connector Pinout

JTAG	BDM Port	PIN			JTAG
TDO	TDO	1	2	/QACK	
TDI	TDI	3	4	/TRST	/TRST
	/QREQ	5	6	+3.3V	
TCK	TCK	7	8	nc	
TMS	TMS	9	10	nc	
	/SRESET	11	12	GND	
	/HRESET	13	14	nc	
	/CHKSTOP_OUT	15	16	GND	
	RxD_SMC1	17	18	GND	
	TxD_SMC1	19	20	GND	

JP1

The BDM port (also called COP header) can be used for debugging. It is supported by major debug tool manufactorers.

Note: The BDM port is not assembled on normal production boards, as it is used only for debug purposes during kernel software development. If it is assembled, the connector JP1 slightly violates the height restrictions for PMC modules, which is 4.5mm at the location of JP1. If installed, JP1 is 5.5mm high.

6.3 Connector JP2: Lattice programming port

Connector JP2 connects the JTAG- or programming-port of the Lattice CPLD device.

Table 12: Lattice programming port

Pin No.	Signal	Signal	Pin No.
1	TCK	nc	2
3	TMS	GND	4
5	TDI	+3.3V	6
7	TDO	GND	8
9	/TRST	nc	10

6.4 Jumper JP3: FLASH Programming Enable Jumper

During normal operation both the main and the fallback FLASH may be (re)programmed any time by the MPC8266. Only in case both FLASH images have been corrupted the following programming procedure applies:

The FLASH programming mode is chosen by installing jumper JP3 and powering up the module. This mode is to be used in order to program a completely empty or corrupted FLASH device. The MPC8266 will read the configuration word from a CPLD device and come up in Core Disabled Mode, and the FLASH will be visible in the window programmed in the MPC8266 from PCI to 60x bus. After having programmed the FLASH, the jumper has to be removed again and power needs to be cycled for the CPU to come out of Power-On-Reset with core enabled. Sample code is available on request.

6.5 PMC Connector P11

Table 13: **PMC Connector P11**

Pin No.	PCI-Signal	PCI-Signal	Pin No.
1	TCK	-12V	2
3	GND	/INT A	4
5	/INT B	/INT C	6
7	/BUSMODE1	+5V	8
9	/INT D	PCI_RSV1	10
11	GND	3.3Vaux	12
13	CLK	GND	14
15	GND	/GNT	16
17	/REQ	+5V	18
19	V (I/O)	AD31	20
21	AD28	AD22	22
23	AD25	GND	24
25	GND	CBE3	26
27	AD22	AD21	28
29	AD19	+5V	30
31	V (I/O)	AD17	32
33	/FRAME	GND	34
35	GND	/IRDY	36
37	/DEVSEL	+5V	38
39	GND	/LOCK	40
41	/SDONE	/SB0	42
43	PAR	GND	44
45	V (I/O)	AD15	46
47	AD12	AD11	48
49	AD09	+5V	50
51	GND	/CBE0	52
53	AD06	AD05	54
55	AD04	GND	56
57	V (I/O)	AD03	58
59	AD02	AD01	60
61	AD00	+5V	62
63	GND	/REQ64	64

Pins for –12V, Vaux, and V(I/O) are not connected to the module. The same applies to JTAG signal TCK and PCI signals /LOCK, /SDONE, /SBO, /INTB, /INTC, /INTD. The PCI bridge chip always drives signals to 3.3V level, but it 5V tolerant.

6.6 PMC Connector P12

Table 14: **PMC Connector P12**

Pin No.	PCI-Signal	PCI-Signal	Pin No.
1	+12V	/TRST	2
3	TMS	TDO	4
5	TDI	GND	6
7	GND	PCI_RSV3	8
9	PCI_RSV	PCI_RSV4	10
11	/BUSMODE2	+3.3V	12
13	/PCIRST	/BUSMODE3	14
15	+3.3V	/BUSMODE4	16
17	/PME	GND	18
19	AD30	AD29	20
21	GND	AD26	22
23	AD24	+3.3V	24
25	IDSEL	AD23	26
27	+3.3V	AD20	28
29	AD18	GND	30
31	AD16	/CBE2	32
33	GND	PCI_RESVD	34
35	/TRDY	+3.3V	36
37	GND	/STOP	38
39	/PERR	GND	40
41	+3.3V	/SERR	42
43	/CBE1	GND	44
45	AD14	AD13	46
47	M66EN	AD10	48
49	AD08	+3.3V	50
51	AD07	PCI_RESV	52
53	+3.3V	PCI_RESV	54
55	PCI_RESV	GND	56
57	PCI_RESV	PCI_RESV	58
59	GND	PCI_RESV	60
61	ACK64	+3.3V	62
63	GND	PCI_RESV	64

Pins for +12V and /BUSMODE2 are not connected to the module. The same applies to JTAG signals TMS and /TRST. JTAG TDI is connected to TDO.

6.7 Pin Assignment of the PMC Connector P14 (PMC I/O)

Table 15: PMC Connector P14

ext. Signal	Pin No.	PCI-Signal	PCI-Signal	Pin No.	ext. Signal
MC	1	I/O	I/O	2	CT_D15
CT_D14	3	I/O	I/O	4	CT_D13
CT_D12	5	I/O	I/O	6	GND
CT_D11	7	I/O	I/O	8	CT_D10
CT_D09	9	I/O	I/O	10	CT_D8
CT_D07	11	I/O	I/O	12	GND
CT_D06	13	I/O	I/O	14	CT_D5
CT_D04	15	I/O	I/O	16	CT_D3
CT_D02	17	I/O	I/O	18	CT_D1
GND	19	I/O	I/O	20	CT_D0
CLKFAIL	21	I/O	I/O	22	/FSYNC
SREF_8K	23	I/O	I/O	24	SCLK
GND	25	I/O	I/O	26	/SCLKx2
SL_4	27	I/O	I/O	28	/C16+
SL_2	29	I/O	I/O	30	SL_3
SL_0	31	I/O	I/O	32	SL_1
NC	33	I/O	I/O	34	NC
NC	35	I/O	I/O	36	NC
/C16-	37	I/O	I/O	38	CT_FRAME_B
CT_FRAME_A	39	I/O	I/O	40	CT_NETREF2
CT_NETREF1	41	I/O	I/O	42	/C4
C2	43	I/O	I/O	44	GND
CT_C8_B	45	I/O	I/O	46	CT_C8_A
CT_D16	47	I/O	I/O	48	CT_D17
CT_D18	49	I/O	I/O	50	CT_D19
GND	51	I/O	I/O	52	CT_D20
CT_D21	53	I/O	I/O	54	CT_D22
CT_D23	55	I/O	I/O	56	CT_D24
GND	57	I/O	I/O	58	CT_D25
CT_D26	59	I/O	I/O	60	CT_D27
CT_D28	61	I/O	I/O	62	CT_D29
CT_D30	63	I/O	I/O	64	CT_D31

The SCbus implemented on the NPMC-8266-OC3 is a sub-set of the H.110 bus. SCbus data lines correspond to H.110 data lines CT_D0 – 15.

6.8 The Front Panel Connectors S1 – S2

The front panel connectors are 8-pin RJ45 connectors. The 4 E1/T1 line interfaces are available on the pins of the front panel connectors S1 and S2. Tables 17 - 18 show the pin assignments.

Table 16: Pin Assignment of the Front-panel Connectors S1 (ISDN)

Pin No.	Signal	Signal	Pin No.
1	TX3+	TX3-	2
3	TX1-	RX1+	4
5	RX1-	TX1-	6
7	RX3+	RX3-	8

Table 17: Pin Assignment of the Front-panel Connectors S2 (ISDN)

Pin No.	Signal	Signal	Pin No.
1	TX4+	TX4-	2
3	TX2-	RX2+	4
5	RX2-	TX2-	6
7	RX4+	RX4-	8

7 NPMC-8266-OC3 Programming Notes

7.1 CPU-Setup

The basic setting of the clocks is done by pulling the MODCK pins during /HRESET. These are programmable through CPLD U13 (BA0-2). There are 5 additional pins (PCIMODCKx) responsible for setting the PLLs, which are also read during /HRESET. The chosen PLL setting is MODCK1-3 = 011b and PCIMODCK0-3 = 0b for a 266/200 MHz CPU version. Whether the PCI clock frequency is 33 MHz or 66 MHz, depends on the status of the PMC /M66EN signal during /HRESET.

7.2 Hard Reset Configuration Word

/RSTCONF is tied to GND, therefore the MPC8266 is the configuration master, i.e. it reads configuration data during the /HRESET - phase from a CPLD. In case an empty FLASH shall be programmed via the PCI bus, the MPC8266 can be put into Core Disabled mode by installing a jumper (JP3).

The configuration data used for normal power-up (not FLASH programming mode) read as follows:

Table 18: Hard Reset Configuration Word (as read from CPLD)

Bit	Name	Value	Description
0	EARB	0b	internal arbiter active
1	EXMC	0b	internal Memory-Controller
2	CDIS	1b	Core disabled
3	EBM	1b	601 compatible bus mode
4-5	BPS	01/10b	Boot Port Size 8/16 bit, depending on JP4
6	CIP	1b	Position of the Vector Table is 0H
7	ISPS	0b	64-bit slave
8-9	L2CPC	10b	L2 Cache pins defined as BADDRx
10-11	DPPC	0b	Data Parity Pins used as IRQ pins
12	rsvd	0b	clear
13-15	ISB	010b	initial internal space base select is 0x0F00.0000
16	BMS	1b	boot from low mem
17	BBD	0b	ABB, DBB Pins defined
18-19	MMR	10b	core / external master requests 2 & 3 masked
20-21	LBPC	01b	PCI bus pins enabled
22-23	APPC	10b	Bank Select function selected
24-25	CS10PC	01b	BCTL1 selected
26	ALD_EN	1b	autoload enabled
27	rsvd	0b	clear
28-31	MODCK_H	0b	PLL configuration, clear

7.2.1 Core Disabled Mode (FLASH programming mode)

In case of FLASH programming mode the ALD_EN bit in the Hard Reset Configuration Word is set to 1b (autoload function, bit 26). In this case, the MPC8266 reads additional information from the CPLD, in order to do some basic register setup. The start address of this block of additional information is always read from address 0x04. The CPLD sets the block start address to be 0x80. The following register setup is performed in core disabled mode for FLASH programming mode:

- SYPCR is written 0xFFFF.FF00 in order to disable the watchdog
- PCI Sub System Device ID is written 0x0603, which is used as N.A.T. board identification code for the **NPMC-8266_OC3**
- PCI Inbound Comparison Mask Register PICMR1 is written to 0x800F.FFE0 in order to request 128KB of PCI memory space for programming mode
- PCI Bus Function register is written 0x0 in order to clear CFG_LOCK and enable PCI access to the bridge
- register OR0 is written 0xFE00.0E84, which reduces the no. of waitstates to 8
- register BR0 is written 0xFE00.1001, which sets the port size to 16 bits data width or to 8 bits data width, depending on the setting of JP4 (refer to chapter 4.3.2)

With these settings FLASH programming via the PCI bus can be performed with the CPU core in disabled mode. After the FLASH programming is completed, jumper JP3 has to be removed again, in order to allow core enabled boot whith the next power-cycle.

7.3 Recommended General Control Register Setup

7.3.1 Register-Setup of the System Clock Control Register (SCCR)

SCCR Bit	Name	Value	Description
Bit 0-28	rsvd	0b	clear
Bit 29	CLPD	0b	CPM does not enter low power mode
Bit 30-31	DFBRG	0b	division factor of 4

7.3.2 Register-Setup of the System Protection Control Register (SYPCR)

SYPCR Bit	Name	Value	Description
Bit 0-15	SWTC	0xFFFF	software watchdog timer count
Bit 16-23	BMT	0xFF	bus monitor timing
Bit 24	PBME	1b	60x bus monitor enabled
Bit 25	LBME	1b	local bus monitor enabled
Bit 26-28	rsvd	0b	clear
Bit 29	SWE	0b	software watchdog disabled
Bit 30	SWRI	1b	watchdog and bus monitors cause soft reset
Bit 31	SWP	1b	software watchdog timer is prescaled

7.3.3 Register-Setup of the Bus Configurations Register (BCR)

BCR Bit	Name	Value	Description
Bit 0	EBM	1b	external bus mode 60x mode
Bit 1-3	APD	011b	address phase delay
Bit 4	L2C	0b	no secondary cache
Bit 5-7	L2D	0b	hit delay, not applicable
Bit 8	PLDP	0b	pipeline max. depth
Bit 9	EAV	1b	full address on 60x bus
Bit 10-11	rsvd	0b	clear
Bit 12	ETM	0b	compatibility mode enable, disabled
Bit 13	LETM	0b	local compatibility mode enable, disabled
Bit 14	EPAR	0b	even parity
Bit 15	LEPAR	0b	local even parity
Bit 16-18	NPQM	111b	non PowerQUICC master
Bit 19-20	rsvd	0b	clear
Bit 21	EXDD	0b	external master delay enabled
Bit 22-26	rsvd	0b	clear
Bit 27	ISPS	0b	internal space port size is 64 bit
Bit 28-31	rsvd	0b	clear

7.3.4 Register-Setup of the 60x Bus Arbiter Configurations Register (PPC_ACR)

P_ACR Bit	Name	Value	Description
Bit 0-1	rsvd	0b	clear
Bit 2	DBGD	0b	DBG asserted with TS
Bit 3	EARB	0b	internal bus arbitration
Bit 4-7	PRKM	0010b	parking master is CPM low request level

7.3.5 Register-Setup of the Local Bus Arbiter Configurations Register (LCL_ACR)

L_ACR Bit	Name	Value	Description
Bit 0	rsvd	0b	clear
Bit 2	DBGD	0b	DBG asserted with TS
Bit 3	EARB	0b	internal bus arbitration
Bit 4-7	PRKM	0110b	parking master is internal core

7.3.6 Register-Setup of the SIU Module Configurations Register (SIUMCR)

SIUMCR Bit	Name	Value	Description
Bit 0	BBD	0b	ABB, DBB selected
Bit 1	ESE	0b	IRQ1 selected
Bit 2	PBSE	0b	parity byte select disabled
Bit 3	CDIS	0b	core enabled
Bit 4-5	DPPC	00b	IRQ function selected
Bit 6-7	L2CPC	10b	BADDRx selected
Bit 8-9	LBPC	1b	PCI bus pins selected
Bit 10-11	APPC	10b	BNKSEL function enabled
Bit 12-13	CS10PC	01b	BCTL1 selected
Bit 14-15	BCTLC	0b	buffer control
Bit 16-17	MMR	0b	no masking of bus requests
Bit 18	LPBSE	0b	local parity disabled
Bit 19-31	rsvd	0b	clear

7.3.7 Register-Setup of the 60x Bus Transfer Status/Control Register (TESCR1)

SCCR Bit	Name	Value	Description
Bit 0-16	not used	0b	clear
Bit 17	DMD	1b	all data errors disabled
Bit 18-31	not used	0b	clear

7.3.8 Register-Setup of the Local Bus Transfer Status/Control Register (L_TESCR1)

SCCR Bit	Name	Value	Description
Bit 0-16	not used	0b	clear
Bit 17	DMD	1b	all data parity errors disabled
Bit 18-31	not used	0b	clear

7.4 Recommended Register Setup of the Memory Controller:

7.4.1 Base Registers BRx:

The base addresses given in the description below are the ones chosen for the OK1 and VxWorks implementations for the NPMC-8266-OC3. They may be altered to suit the user's needs.

BRx: Base Register of the corresponding CS; CS settings as described in Table 3 above.

BR0 Bit	Name	Value	Description
Bit 0-16	BA	<address>	base address <address>, FLASH
Bit 17-18	rsvd	0b	clear
Bit 19-20	PS	10b	port size 16 bit
Bit 21-22	DECC	0b	ECC disabled
Bit 23	WP	0b	R/W
Bit 24-26	MS	0b	default, 601 bus
Bit 27	EMEMC	0b	memory controller active
Bit 28-29	ATOM	0b	no atomic operations
Bit 30	DR	0b	no data pipelining
Bit 31	V	1b	valid bank

BR1 not used.

BR2 Bit	Name	Value	Description
Bit 0-16	BA	<address>	base address <address>, SDRAM CS0
Bit 17-18	rsvd	0b	clear
Bit 19-20	PS	0b	port size 64 bit
Bit 21-22	DECC	0b	ECC disabled
Bit 23	WP	0b	R/W
Bit 24-26	MS	010b	SDRAM, 601 bus
Bit 27	EMEMC	0b	memory controller active
Bit 28-29	ATOM	0b	no atomic operations
Bit 30	DR	0b	no data pipelining
Bit 31	V	1b	valid bank

The settings of BR2 and BR3 are suitable for the default 32 MB SODIMM module installed. The default module uses only one CS, hence the programming of BR3/OR3 is not necessary.

BR3 Bit	Name	Value	Description
Bit 0-16	BA	<address>	base address <address>, SDRAM CS1
Bit 17-18	rsvd	0b	clear
Bit 19-20	PS	0b	port size 64 bit
Bit 21-22	DECC	0b	ECC disabled
Bit 23	WP	0b	R/W
Bit 24-26	MS	010b	SDRAM, 601 bus
Bit 27	EMEMC	0b	memory controller active
Bit 28-29	ATOM	0b	no atomic operations
Bit 30	DR	0b	no data pipelining
Bit 31	V	0b	invalid bank

BR4 Bit	Name	Value	Description
Bit 0-16	BA	<address>	base address <address>, Reset register
Bit 17-18	rsvd	0b	clear
Bit 19-20	PS	01b	port size 8 bit
Bit 21-22	DECC	0b	ECC disabled
Bit 23	WP	0b	R/W
Bit 24-26	MS	0b	GPCM, 601 bus
Bit 27	EMEMC	0b	memory controller active
Bit 28-29	ATOM	0b	no atomic operations
Bit 30	DR	0b	no data pipelining
Bit 31	V	1b	valid bank

BR5 Bit	Name	Value	Description
Bit 0-16	BA	<address>	base address <address>, TSI
Bit 17-18	rsvd	0b	clear
Bit 19-20	PS	01b	port size 8 bit
Bit 21-22	DECC	0b	ECC disabled
Bit 23	WP	0b	R/W
Bit 24-26	MS	0b	GPCM, 601 bus
Bit 27	EMEMC	0b	memory controller active
Bit 28-29	ATOM	0b	no atomic operations
Bit 30	DR	0b	no data pipelining
Bit 31	V	1b	valid bank

BR6 Bit	Name	Value	Description
Bit 0-16	BA	<address>	base address <address>, QuadFALC
Bit 17-18	rsvd	0b	clear
Bit 19-20	PS	01b	port size 8 bit
Bit 21-22	DECC	0b	ECC disabled
Bit 23	WP	0b	R/W
Bit 24-26	MS	0b	GPCM, 601 bus
Bit 27	EMEMC	0b	memory controller active
Bit 28-29	ATOM	0b	no atomic operations
Bit 30	DR	0b	no data pipelining
Bit 31	V	1b	valid bank

BR7 - 11 not used.

7.4.2 Option Registers ORx

The address masks given in the description below are the ones chosen for the OK1 and VxWorks implementations for the NPMC-8260-E1. They may be altered to suit the user's needs.

ORx: Option Registers of the corresponding CS, CS settings as described in Table 3 above.

OR0 Bit	Name	Value	Description
Bit 0-16	AM	FF00.0H	address mask, size of the CS range, 16 MB
Bit 17-18	rsvd	0b	clear
Bit 19	BCTLD	0b	BCTLx enabled (R/W control)
Bit 20	CSNT	1b	CS/WE timing parameter
Bit 21-22	ACS	11b	CS timing parameter
Bit 23	rsvd	0b	clear
Bit 24-27	SCY	1011b	11 WS = 13 clock cycles = 170ns access time
Bit 28	SETA	0b	internal TA/PSDVAL generation
Bit 29	TRLX	0b	normal timing
Bit 30	EHTR	0b	normal timing
Bit 31	rsvd	0b	clear

OR1 not used.

OR2 Bit	Name	Value	Description
Bit 0-11	SDAM	FE0H	SDRAM address mask, size of the CS range, 32 MB
Bit 12-16	LSDAM	0H	lower SDRAM address mask
Bit 17-18	BPD	01b	banks per device, default: 4 banks
Bit 19-21	ROWST	0010b	row start address bit (from SDRAM EEPROM), see also DRTYPEx programming
Bit 22	rsvd	0b	clear
Bit 23-25	NUMR	011b	number of row address lines (from SDRAM EEPROM)
Bit 26	PMSEL	0b	page mode select back to back
Bit 27	IBID	0b	internal bank interleave activated
Bit 28-31	rsvd	0b	clear

The settings of OR2 and OR3 are suitable for the default 32 MB SODIMM module installed. The default module uses only one CS, hence the programming of BR3/OR3 is not necessary.

OR3 Bit	Name	Value	Description
Bit 0-11	SDAM	FE0H	SDRAM address mask, size of the CS range, 32 MB
Bit 12-16	LSDAM	0H	lower SDRAM address mask
Bit 17-18	BPD	01b	banks per device, default: 4 banks
Bit 19-21	ROWST	0010b	row start address bit (from SDRAM EEPROM), see also DRTYPEx programming
Bit 22	rsvd	0b	clear
Bit 23-25	NUMR	011	number of row address lines (from SDRAM EEPROM)
Bit 26	PMSEL	0b	page mode select back to back
Bit 27	IBID	0b	internal bank interleave activated
Bit 28-31	rsvd	0b	clear

OR4 Bit	Name	Value	Description
Bit 0-16	AM	FFFF.0H	address mask, size of the CS range, 64 KB
Bit 17-18	rsvd	0b	clear
Bit 19	BCTLD	0b	L_WR enabled (R/W control)
Bit 20	CSNT	0b	CS/WE timing parameter
Bit 21-22	ACS	11b	CS timing parameter
Bit 23	rsvd	0b	clear
Bit 24-27	SCY	0101b	5 WS = 7 clock cycles = 80ns access time
Bit 28	SETA	0b	internal TA/PSDVAL generation
Bit 29	TRLX	1b	relaxed timing
Bit 30	EHTR	1b	extended hold time
Bit 31	rsvd	0b	clear

OR5 Bit	Name	Value	Description
Bit 0-16	AM	FFFF.0H	address mask, size of the CS range, 64 KB
Bit 17-18	rsvd	0b	clear
Bit 19	BCTLD	0b	L_WR enabled (R/W control)
Bit 20	CSNT	0b	CS/WE timing parameter
Bit 21-22	ACS	11b	CS timing parameter
Bit 23	rsvd	0b	clear
Bit 24-27	SCY	0101b	5 WS = 7 clock cycles = 80ns access time
Bit 28	SETA	0b	internal TA/PSDVAL generation
Bit 29	TRLX	1b	relaxed timing
Bit 30	EHTR	1b	extended hold time
Bit 31	rsvd	0b	clear

OR6 Bit	Name	Value	Description
Bit 0-16	AM	FFFF.0H	address mask, size of the CS range, 64 KB
Bit 17-18	rsvd	0b	clear
Bit 19	BCTLD	0b	L_WR enabled (R/W control)
Bit 20	CSNT	0b	CS/WE timing parameter
Bit 21-22	ACS	11b	CS timing parameter
Bit 23	rsvd	0b	clear
Bit 24-27	SCY	0101b	5 WS = 7 clock cycles = 80ns access time
Bit 28	SETA	0b	internal TA/PSDVAL generation
Bit 29	TRLX	1b	relaxed timing
Bit 30	EHTR	1b	extended hold time
Bit 31	rsvd	0b	clear

OR7 - 11 not used.

7.4.3 Configuration for SDRAM Register Setup

The correlation between address lines to be multiplexed and the programmierung of the signals DRTYPEx and Bank Select (BAx) is as follows:

DRTYPEx settings are related to the SODIMM SDRAM row/culomn organisation. The following table shows which is the highest column address to be multiplexed, which address lines have to be put out by the BAx lines (BA0 is not connected), and how SDA10 should be programmed according to the setting of DRTYPEx:

DRTYPE1	DRTYPE0	highest col. addr. to be muxed	BA1	BA2	SDA10
0	0	SDA7	PB_A19	PB_A20	PB_A8
0	1	SDA8	PB_A18	PB_A19	PB_A7
1	0	SDA9	PB_A17	PB_A18	PB_A6
1	1	SDA11	PB_A16	PB_A17	PB_A5

DRTYPEx are programmable by Port pins of the MPC8280.
DRTYPE0 is PC5, DRTYPE1 is PC4.

7.4.4 SDRAM Mode Register PSDMRx

PSDMR Bit	Name	Value	Description
Bit 0	PBI	1b	page-based Interleave
Bit 1	RFEN	1b	refresh necessary
Bit 2-4	OP	000b	SDRAM operation
Bit 5-7	SDAM	010b	depending on SDRAM parameters and on DRTYPEx
Bit 8-10	BSMA	110b	depending on SDRAM parameters and on DRTYPEx
Bit 11-13	SDA10	010b	depending on SDRAM parameters and on DRTYPEx (see table below)
Bit 14-16	RFRC	110b	depending on SDRAM parameters
Bit 17-19	PRETOACT	100b	depending on SDRAM parameters
Bit 20-22	ACTTORW	100b	depending on SDRAM parameters
Bit 23	BL	0b	burst length is 4
Bit 24-25	LDOTOPRE	10b	depending on SDRAM parameters
Bit 26-27	WRC	11b	depending on SDRAM parameters
Bit 28	EAMUX	1b	external address multiplexer
Bit 29	BUFCMD	0b	normal timing
Bit 30-31	CL	10b	depending on SDRAM parameters

7.4.5 PSRT 60x Bus-Assigned SDRAM Refresh Timer Register

PSRT Bit	Name	Value	Description
Bit 0-7	PSRT	20H	timer value of 32 for prescaler 64

7.4.6 MPTPR Memory Refresh Timer Prescaler Register

MPTPR Bit	Name	Value	Description
Bit 0-7	PSRT	40H	prescaler value 64
Bit 8-15	rsvd	0b	clear

7.4.7 UPM Machine Mode Register MxMR

UPMs are not used in this version. If UPMs are to be used, take the restriction of bus frequency and UPM usage for some MPC8266 masks and versions into account.

7.5 Setup of the Serial Interface

7.5.1 RS232 Debug Interface

The programming of the RS232 serial debug interface is performed through SMC1 (PD8, PD9).

7.5.2 I^2C Interface

The I^2C interface is connected to port pins PD30 (Clk) and PD31 (Data). The EEPROM on the SDRAM SODIMM module has address 0 and should be read and analyzed before initialising the SDRAM machine, in order to be able to setup the SDRAM machine, the external logik (DRTYPEx for U13), and the SDRAMs themselves. The address of the EEPROM U10 used for storage of board-specific parameters is 4. The control code (1^{st} 4 bits of the address) for the 24Cxx EEPROM is 1010b, which results in address $50 for the SODIMM EEPROM and in address $54 for the parameter EEPROM.

7.6 Definition of the Multi-Function Pins

Table 19: Definition of the Multi-Function Pins

Pin Name	Pin Function on the NPMC-8266-OC3
DBB/IRQ3	DBB
DP(0-7)/misc.	IRQx
GBL/IRQ1	GBL, not used
CI/BADDR29/IRQ2	BADDR29
WT/BADDR30/IRQ3	BADDR30
L2_HIT/IRQ4	L2_HIT, not used
CPU_BG/BADDR31/IRQ5	BADDR31
CS10/BCTL1/DBG_DIS	BCTL1
CS11/AP0	NC
PWE(0-7)/PSDDQM(0-7)/PBS(0-7)	PSDDQM(0-7)
PSDA10/PGPL0	PSDA10
PSDWE/PGPL1	PSDWE
POE/PSDRAS/PGPL2	PSDRAS
PSDCAS/PGPL3	PSDCAS
PGTA/PUPMWAIT/PGPL4/PPBS	PGTA
PSDAMUX/PGPL5	PSDAMUX
IRQ0/NMIOUT	IRQ0
IRQ7/INTOUT/APE	INTOUT, not used
MODCKx/Apx/TCx/BNKSELx	BNKSELx

Appendix A: Reference Documentation

[1] Motorola Inc., MPC8260 PowerQUICC II User's Manual, 5/1999, Rev. 0
[2] Motorola Inc., MPC8265 User's Manual Addendum, 11/2002, Rev. 0.4
[3] Motorola Inc., MPC8266 User's Manual Addendum, 7/2002, Rev. 1.2
[4] OKI Inc., ML53812-2 Universal Timeslot Interchange, Preliminary Data Sheet, 1996, Rev. 1.3
[5] Infineon, PEB22554 E1/T1/J1 Framer / Transceiver, 7/2000, DS1
[6] PMC Sierra, PM5384 S/UNI-1x155 SATURN User Network Interface (1x155) Telecom Standard Product, 4/2002, Rev. 4
[7] N.A.T. GmbH, NFAPI Manual, 1999, Rev.1.7

Appendix B: Document's History

Revision	Date	Description	Author
1.0	28.01.2003	initial revision	ga
1.1	30.04.2003	P13 removed	ga
1.2	05.09.2003	figure 6 corrected	ga
1.3	08.07.2004	chapter 4.3 added, chapter chapter 6.2 revised	ga
1.4	21.03.2006	added '5V intolerance note' to chapter 2	ga
1.5	06.06.2007	chapter 2.3 added	ga