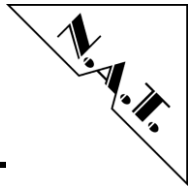

NcPCI-XLINK
Technical Reference Manual V1.0
HW Revision 1.0

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Note:

The release of the Hardware Manual is related to a particular HW board revision given in the document title. For earlier hardware revisions please contact N.A.T. for the relevant Hardware Manual release.

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Conventions

If not otherwise specified, addresses and memory maps are written in hexadecimal notation, identified by *0x*.
Table 1 gives a list of the abbreviations used in this document:

Table 1: List of used Abbreviations

Abbreviation	Description
b	Bit, binary
B	byte
cPCI	CompactPCI
nc	not connected
PCI	Peripheral Component Interconnect
PCIe	PCI Express
PICMG	PCI Industrial Computer Manufacturers Group
OS	Operating System

1 Introduction

The **NcPCI-XLINK** is a high performance 32-bit, 33 MHz PCI Card. It can be plugged into any master PCI slot supporting PCI standards with 3.3V signalling. The PCI interface is 5V tolerant.

The **NcPCI-XLINK** connects a one-lane PCI Express External Cable Interface Connector on the front panel to a passive PCI backplane through programmable ReDriver circuitry and a PCIe → PCI bridge device.

The **NcPCI-XLINK** is member of a family of XLINK boards which enable the connection of different system platforms via a PCI Express External Cable Interface. Typically one system will be a master system containing a processor card and the second system will be a slave system which does not contain a processor card and is controlled by the master system. Examples of other XLINK products are the **MAMC-XLINK** and the **NcPCIe-XLINK**.

1.1 Installation

The **NcPCI-XLINK** is the master card in the PCI system and should be installed into the master slot of a passive PCI backplane. Normally the processor card is installed into this slot. This combination produces a slave PCI system (no processor card). The card should not be installed in a standard (slave) slot, as the **NcPCI-XLINK** drives clock and arbitration signals for the PCI bus and thus has a PCI connector pinning that differs from that of a standard PCI card.

The **NcPCI-XLINK** is a slave cable interface, i.e. it does not provide master functionality for the cable interface such as clock and management signals. When connecting it to another XLINK board via the cable, the other board must have master functionality for the cable interface! This board is usually a slave board in the system in which it is installed. An example of a board with this kind of master functionality for the cable interface is the **MAMC-XLINK**.

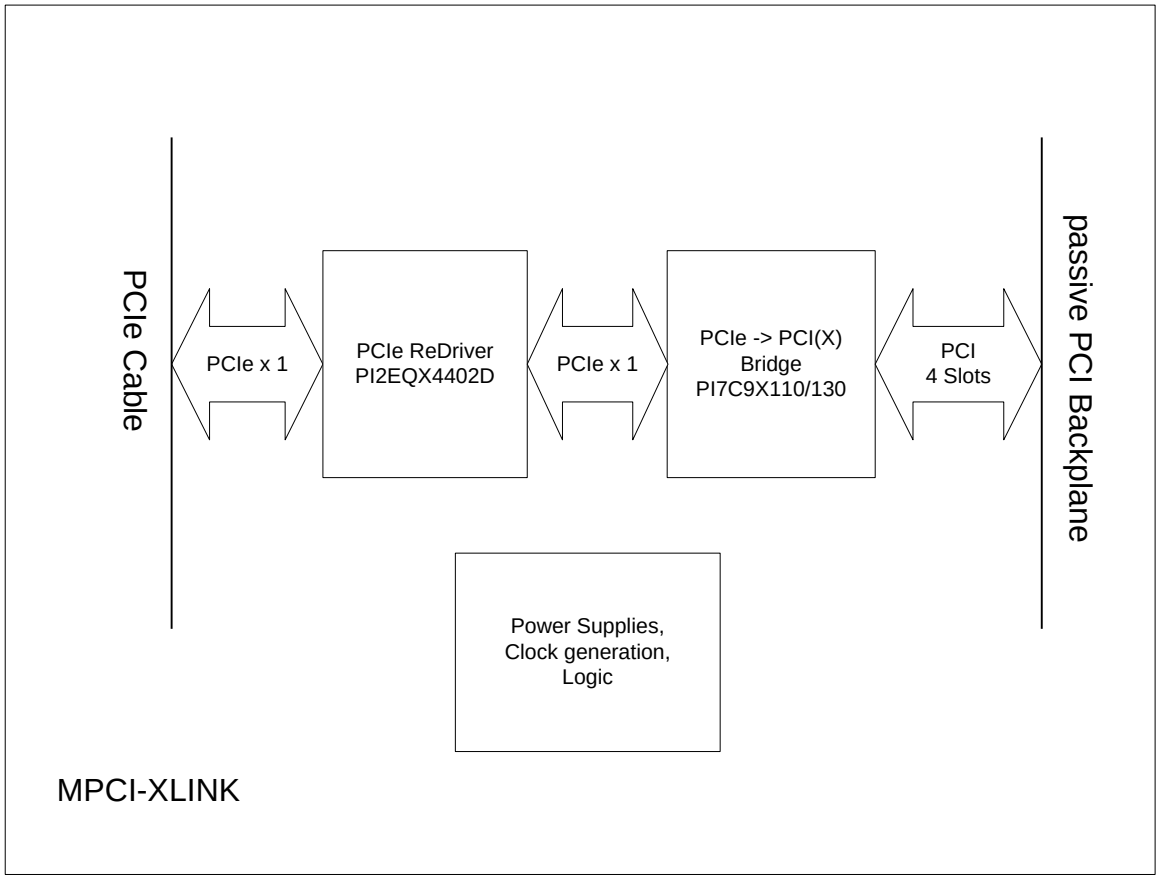
The master cable interface, e.g. the **MAMC-XLINK**, has to sense the presence of the slave interface of the **NcPCI-XLINK**. Typically this is performed by firmware after Power-Up. In order to sense the presence of the **NcPCI-XLINK** correctly, the PCI system should be powered up first. A rescan of the cable link can be performed at any time by user software.

1.2 Block Diagram

The **NcPCI-XLINK** has the following major features implemented on-board:

- 32 bit 33 MHz PCI Interface Rev. 3.0 to PCI backplane
- 1 Lane PCI Express External Cable Interface Rev. 1.0 to front panel
- ReDriver circuitry for conditioning the PCIe signals
- PCIe → PCI Bridge with master slot support

Figure 1: NcPCI-XLINK Block Diagram



1.3 Board Features

- **PCI Master Slot Interface**

  The **NcPCI-XLINK** includes a PCI Master Slot Interface on the edge connector. The PCI card interfaces to the master slot of a passive PCI backplane. It supports 4 standard PCI slots by providing individual PCI clock and arbitration signals. The implementation of the PCI Master Slot Interface conforms to PICMG 1.0 R2.0 PCI-ISA Card Edge Connector for Single Board Computer. It implements only the PCI part of the specification, not the ISA part.

- **PCI Express External Cable Interface**

  The **NcPCI-XLINK** has a single lane PCI Express External Cable Interface using a front panel cable connector. The implementation of the PCI Express External Cable Interface conforms to the PCI Express External Cabling Specification, Rev. 1.0. The transfer data rate is 2.5GB/s.

- **PCIe → PCI Bridge with Master Slot Support**

  The **NcPCI-XLINK** implements an PCIe → PCI Bridge with master slot support, which conforms to the PCI-to-PCI Bridge Architecture Specification. Therefore with standard OSes like Windows or Linux no special drivers are needed.

- **ReDriver Circuitry**

  The **NcPCI-XLINK** includes ReDriver circuitry in order to guarantee PCIe signal quality at the receiver portion of the PCI Express External Cable Interface.

- **Clock Selection**

  The **NcPCI-XLINK** offers the choice to select between a local PCIe clock and the PCI Express External Cable Interface, which is defined in the PCI Express External Cabling Specification.

1.4 Board Specification

Table 2: NcPCI-XLINK Features

PCI Form Factor	standard PCI short from factor, 32 bit, 3.3V signalling, 5V tolerant	
Front-I/O	Single lane PCI Express External Cable Connector, 2.5GB/s data rate	
Firmware	IPMI firmware on request	
Power Consumption	V(I/O) 0.1A max. (V(I/O) can be either 5V or 3.3V) 3.3V 0.5A max.	
Environmental Conditions	Temperature (operating):	0°C to +70°C with forced cooling
	Temperature (storage):	-40°C to +85°C
	Humidity:	10 % to 90 % rh noncondensing
Standards Compliance	PCI Express Base Specification Rev. 2.0	
	PCI Express External Cabling Specification, Rev. 1.0	
	PCI Local Bus Specification, Revision 3.0, February 3, 2004	
	PCI-to-PCI Bridge Architecture Specification, Revision 1.2	
	PICMG 2.5 R1.0	
	IPMI Specification v2.0 Rev. 1.0	

Note:

The PCI bridge always drives signals to 3.3V level (3.3V signalling), but is 5V tolerant.

2 Installation

2.1 Safety Note

To ensure correct operation of the **NcPCI-XLINK** take the following precautions before handling the board.

CAUTION

Electrostatic discharge and incorrect board installation and removal can damage circuits or shorten their life.

- Before installing or removing the **NcPCI-XLINK**

- Check all installed boards and modules for steps that you have to take before turning on or off the power.
  - Take those steps.
  - Finally turn off the power.

- Before touching integrated circuits take all the required precautions for handling electrostatic devices.
- When operating the board in areas of strong electromagnetic radiation ensure that the module
  - is screwed to the front panel or rack
  - and shielded by a screened enclosure

2.2 Installation Prerequisites and Requirements

IMPORTANT

Before powering up

- check this section for installation prerequisites and requirements

2.2.1 Requirements

The installation requires

- a passive PCI backplane to connect to the **NcPCI-XLINK**
- power supply

2.2.2 Power Supply

The power supply for the **NcPCI-XLINK** must meet the following specifications:

- +3.3V 0.5A
- V(I/O) 0.1A (V(I/O) can be either 5V or 3.3V)

2.2.3 Automatic Power Up

In the following situations the **NcPCI-XLINK** will automatically be reset and proceed with a normal power up.

Voltage sensors

The voltage sensor generates a reset

- when +3.3V voltage level drops below 3.08V

or when the upstream (cable master) XLINK board signals CPERST#.

2.2.4 Thermal Considerations

The **NcPCI-XLINK** can be operated in a temperature range of 0°C to +70°C.

2.3 Statement on Environmental Protection

2.3.1 Compliance to RoHS Directive

Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) states that all electrical and electronic equipment being put on the European market after June 30th, 2006 may contain lead, mercury, hexavalent chromium, polybrominated biphenyls (PBB) and polybrominated diphenyl ethers (PBDE) and cadmium in maximum concentration values of 0.1% respective 0.01% by weight in homogenous materials only.

As these hazardous substances are currently used with semiconductors, plastics (i.e. semiconductor packages, connectors) and soldering tin, any hardware product is affected by the RoHS directive if it does not belong to one of the groups of products exempted from the RoHS directive.

Although many of the N.A.T. hardware products are exempt from the RoHS directive it is the policy of N.A.T. to produce compliant products wherever possible. Since January 31st, 2005, N.A.T. has stipulated RoHS compliant components from its suppliers. RoHs compliance is also mandatory in the production process.

2.3.2 Compliance to WEEE Directive

Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) mandates that manufacturers of electrical and electronic equipment which is put onto the European market have to contribute to the reuse, recycling and other forms of recovery of such waste. This directive makes reference to the Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS).

Although the main focus is on household use, the directive also affects business-to-business relationships. The directive is quite restrictive on how household waste has to be handled by the supplier/manufacturer; however, it allows a greater flexibility in business-to-business relationships. This is due to the fact that industrial electrical and electronic products are commonly integrated into larger and more complex environments or systems that cannot easily be dismantled when it comes to their disposal at the end of their life cycle.

As N.A.T. products are sold solely to industrial customers, at the time of purchase the customer agrees to take the responsibility for a WEEE compliant disposal of the used N.A.T. product. All N.A.T. products are marked according to the directive with a crossed out bin to indicate that these products within the European Community must not be disposed with ordinary waste.

If you have any questions on the policy of N.A.T. regarding the Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) or the Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) please contact N.A.T. by phone or e-mail.

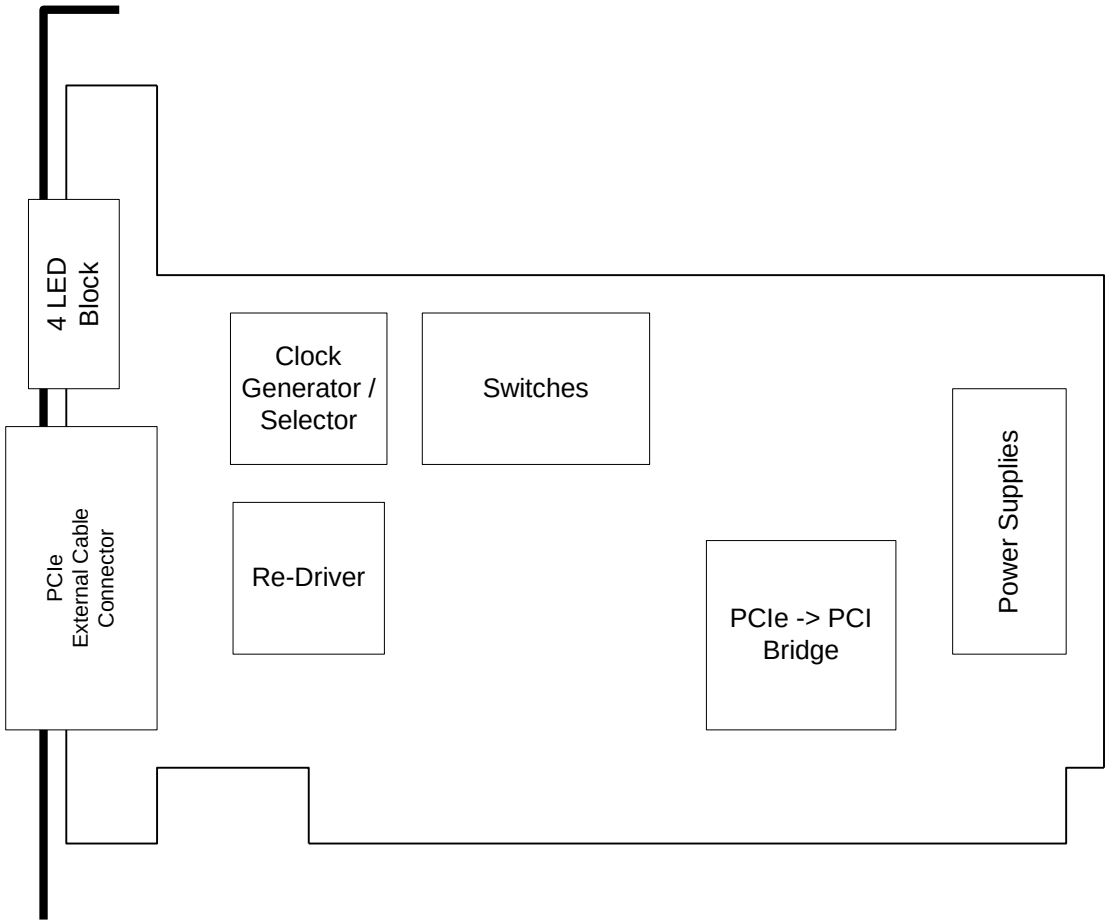
2.3.3 Compliance to CE Directive

Compliance to the CE directive is declared. A ‘CE’ sign can be found on the PCB.

2.4 Location Overview

Figure 3 "Location diagram of the **NcPCI-XLINK**" shows the position of major components. Some of the components may not be populated depending on the board version.

Figure 2: Location Diagram of the NcPCI-XLINK



3 Functional Blocks

The **NcPCI-XLINK** can be divided into a number of functional blocks, which are described in the following paragraphs.

3.1 ReDriver Circuitry

The **NcPCI-XLINK** includes ReDriver circuitry to guarantee PCIe signal quality at the receiver portion of the PCI Express External Cable Interface. There are different length cables available which comply to the PCI Express External Cable Interface Specification. Although the specification does not specify individual cable lengths, transmission characteristics require that the cable length should not exceed 7m. The Pericom PI2EQX4402D ReDriver device installed on the **NcPCI-XLINK** allows the user to adapt transmission charateristics to different cable lengths. As cable types and lengths will differ it is not possible to give specific settings for the ReDriver under all conditions. The user may need to adjust the settings if the default settings do not result in satisfactory performance. With the **NcPCI-XLINK** this can be done using switch settings. Please refer to chapters 5.4 and 5.5 for a more detailed explanation. The PI2EQX4402D ReDriver device implements four unidirectional ports, two of which are used on the **NcPCI-XLINK**. Port B is used to drive the PCIe line from the PCIe → PCI bridge to the PCI Express Cable Interface connector, Port C is used to drive the PCIe line from the PCI Express Cable Interface connector to the PCIe → PCI bridge. Ports A and D are permanently disabled.

3.2 PCIe → PCI Bridge with Master Slot Support

The **NcPCI-XLINK** implements a Pericom PI7C9C111SL PCIe → PCI Bridge with master slot support, which conforms to the PCI-to-PCI Bridge Architecture Specification. The PI7C9X111SL is a PCIe → PCI/PCI-X bridge and is compliant with the PCI Express Base Specification, Revision 1.1; the PCI Express Card Electromechanical Specification, Revision 1.1; the PCI Local Bus Specification, Revision 3.0 and the PCI Express to PCI/PCI-X Bridge Specification, Revision 1.0. It supports transparent mode operation and forward and reverse bridging. In forward bridging mode it has a single PCI Express upstream port and a 32-bit PCI downstream port. In reverse bridging mode it has a 32-bit PCI upstream port and a single PCI Express downstream port. On the **NcPCI-XLINK** the bridge is used in forward mode. The PI7C9X111SL configuration registers are backward compatible with existing PCI bridge software and firmware. No modification of PCI bridge software or firmware is needed for normal operation. Please refer to chapter 4.1 for a more detailed explanation.

3.3 PCIe Clock Interface

The PCIe clock can be derived either from the clock transmitted through the PCI Express External Cable Interface, or from an internal oscillator. Both clock sources are routed to a multiplexer which allows selecting the clock source of the PCIe → PCI bridge to be either from the PCI Express External Cable Interface clock, or from the internal differential 100 MHz reference clock.
The **NcPCI-XLINK** is always clock slave of the PCI Express External Cable Interface, i.e. the clock is received from the cable interface, but not transmitted to it.

3.4 Cable Interface Control Signals

The PCI Express External Cable Interface implemented on the **NcPCI-XLINK** supports the following Cable Interface control signals:

CPERST#, CPRSNT#, CWAKE#, CPWRON

For definition, usage, sensing, and programming of these control signals please refer to chapter 4.4 and to the PCI Express External Cable Interface Specification.

3.5 I^2C Device

There is an I^2C device on the **NcPCI-XLINK**, which is connected to the PCIe → PCI bridge's I^2C bus. This EEPROM can be used for storing setup imformation for the PCIe → PCI bridge after Power-Up, and/or for storage of board-specific information. The EEPROM is of the type 24C02 . The address of the EEPROM is 0x0. By default, the I^2C device 24C02 is not programmed. The bridge initialises with default register values.

4 Hardware Description

4.1 Definition of PI7C9X111SL GPIO Pins

PI7C9X111SL GPIO pins are used to drive the front panel LEDs 3 and 4. In detail:

Table 3: ATmega645 Port Pin Usage (Port A)

Signal Function	PI7C9X111SL GPIO Pin	Description
not used	GPIO3	*pin is unconnected*
not used	GPIO2	*pin is unconnected*
LED4	GPIO1	controls LED 4 on the front panel LED block
LED3	GPIO0	controls LED 3 on the front panel LED block

4.2 Front Panel LEDs

There is a 4 LED block located above the PCI Express External Cable connector. LEDs 1 and 2 of this block show the link status of the ReDriver PCIe lines. LEDs 3 and 4 are programmable by the user.

The programmable LEDs are controlled by GPIO0 (LED 3) and GPIO1 (LED 4) pins of the PCIe → PCI bridge device. For further information on how to program these LEDs please refer to the PI7C9X111SL PCI Express-to-PCI Reversible Bridge Data Book, or ask N.A.T. for further assistance. The LEDs are reserved for user applications and not programmed by standard XLINK interface firmware.

4.3 Selecting the PCIe Clock Source

The PCIe clock can be derived either from the clock transmitted through the PCI Express External Cable Interface, or from an internal oscillator. Both clocks are routed to a multiplexer which allows selecting the clock source for the PCIe → PCI bridge to be from either the PCI Express External Cable Interface clock, or from the internal differential 100 MHz reference clock. Selection of the clock source is by position 8 of switch SW2. Switch SW2 position 8 “on” = internal oscillator, switch “off” = PCI Express External Cable Interface clock.

By default, the PCI Express Cable Interface clock is selected.

4.4 PCI Express External Cable Interface Control Signals

The PCI Express External Cable Interface control signals **CPERST#, CPRSNT#, CWAKE#, CPWRON** are controlled by firmware of the upstream XLINK master board.

CPERST# is sent downstream to the PCI Express External Cable Interface by the upstream XLINK master board. Upon reception of **CPERST#** active the PCIe → PCI bridge on the **NcPCI-XLINK** generates PCIRST# for the local PCI bus, in order to reset the entire system.

By driving **CPRSNT#** "low" the downstream system indicates to the upstream system that it has been powered up and is functional. This signal is sensed by the upstream XLINK master board. The **NcPCI-XLINK** drives this signal active when the local voltage supervisor senses power is ok.

By driving **CWAKE#** "low" the downstream system indicates to the upstream system that it shall power up. This function is optional and not implemented.

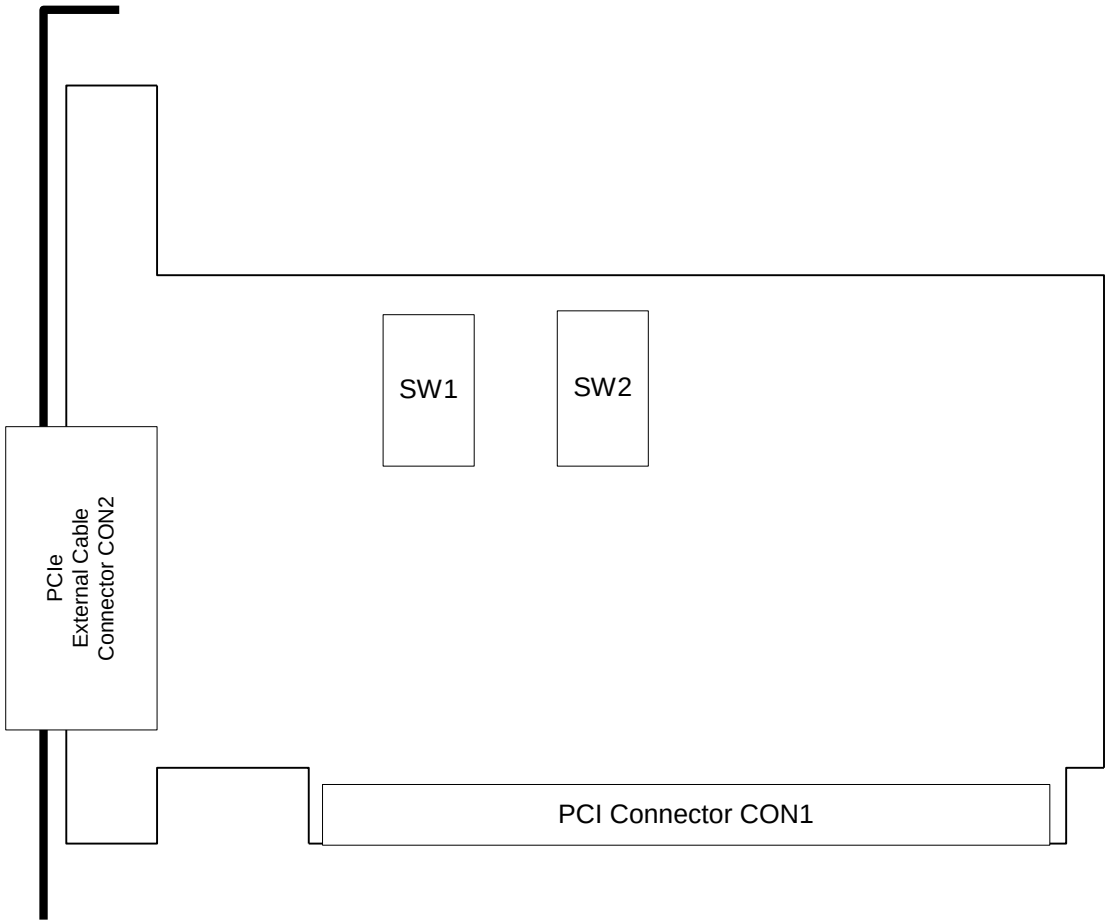
CPWRON# is sent downstream the PCI Express External Cable Interface by the upstream XLINK master board, in order to tell the downstream system that it shall power up. This function is optional and not implemented.

For further information on how to handle these control signals please refer to the PCI Express External Cable Interface Specification and contact N.A.T. GmbH.

5 Connectors and Switches

5.1 Connector Overview

Figure 3: Connectors of the NcPCI-XLINK



Please refer to the following tables to look up the connector pin assignment of the **NcPCI-XLINK**.

5.2 Compact PCI Backplane Connectors

The Compact PCI backplane connectors are 2 6-row connectors J1 A – F and J2 A – F. The 7th row Z does not connect to pins, but is just for shielding and completely connected to GND

5.2.1 Compact PCI Backplane Connector J1

Table 4: Compact PCI Backplane Connector J1 Rows A – C

Pin No.	Row A PCI-Signal	Row B PCI-Signal	Row C PCI-Signal
1	5V	-12V	nc (PD)**
2	nc (PD)**	5V	nc (PU)**
3	/INTA	/INTB	/INTC
4	nc	/HEALTHY	V(I/O)_L
5	nc	nc	/RST
6	/REQ0*	GND	3.3V_L
7	AD30	AD29	AD28
8	AD26	GND	V(I/O)
9	/C/BE3	IDSEL	AD23
10	AD21	GND	3.3V
11	AD18	AD17	AD16
12	Key Area		
13			
14			
15	3.3V	/FRAME	/IRDY
16	/DEVSEL	GND	V(I/O)
17	3.3V	nc	nc
18	/SERR	GND	3.3V
19	3.3V	AD15	AD14
20	AD12	GND	V(I/O)_L
21	3.3V	AD9	AD8
22	AD7	GND	3.3V_L
23	3.3V	AD4	AD3
24	AD1	5V	V(I/O)
25	5V	/REQ64	/ENUM

* /REQ0 in system slot, /REQ in peripheral slot
** connected to 4K7 Pull-Up / Pull-Down in system slot, nc in peripheral slot

Table 5: Compact PCI Backplane Connector J1 Rows D – F

Pin No.	Row D PCI-Signal	Row E PCI-Signal	Row F PCI-Signal
1	+12V	5V	GND
2	nc	nc (PU)**	GND
3	5V_L	/INTD	GND
4	INTP	INTS	GND
5	GND_L	/GNT0*	GND
6	CLK	AD31	GND
7	GND_L	AD27	GND
8	AD25	AD24	GND
9	GND_L	AD22	GND
10	AD20	AD19	GND
11	GND_L	/C/BE2	GND
12	Key Area		
13			
14			
15	/BD_SEL	/TRDY	GND
16	/STOP	/LOCK	GND
17	GND_L	/PERR	GND
18	PAR	/C/BE1	GND
19	GND_L	AD13	GND
20	AD11	AD10	GND
21	M66EN	/C/BE0	GND
22	AD6	AD5	GND
23	5V_L	AD2	GND
24	AD0	/ACK64	GND
25	3.3V	5V	GND

* /GNT0 in system slot, /GNT in peripheral slot

** connected to 4K7 Pull-Up / Pull-Down when assembled for and located in system slot, nc in peripheral slot

5.2.2 Compact PCI Backplane Connector J2

Table 6: Compact PCI Backplane Connector J2 Rows A – C

Pin No.	Row A PCI-Signal	Row B PCI-Signal	Row C PCI-Signal
1	nc / CLK1**	GND	/REQ1*
2	nc / CLK2**	nc / CLK3**	/SYSEN
3	nc / CLK4**	GND	/GNT3*
4	V(I/O)	nc	/C/BE7
5	/C/BE5	GND	V(I/O)
6	AD63	AD62	AD61
7	AD59	GND	V(I/O)
8	AD56	AD55	AD54
9	AD52	GND	V(I/O)
10	AD49	AD48	AD47
11	AD45	GND	V(I/O)
12	AD42	AD41	AD40
13	AD38	GND	V(I/O)
14	AD35	AD34	AD33
15	nc	GND	/FAL
16	nc	nc	/DEG
17	nc	GND	/PRST
18	nc	GND	nc
19	GND	GND	nc
20	nc / CLK5**	GND	nc
21	nc / CLK6**	GND	nc
22	GA4	GA3	GA2

* driven only when assembled for and located in system slot
** connected only when assembled for and located in system slot, nc in peripheral slot

Table 7: Compact PCI Backplane Connector J2 Rows D – F

Pin No.	Row D PCI-Signal	Row E PCI-Signal	Row F PCI-Signal
1	/GNT1*	/REQ2*	GND
2	/GNT2*	/REQ3*	GND
3	/REQ4*	/GNT4*	GND
4	GND	/C/BE6	GND
5	/C/BE4	PAR64	GND
6	GND	AD60	GND
7	AD58	AD57	GND
8	GND	AD53	GND
9	AD51	AD50	GND
10	GND	AD46	GND
11	AD44	AD43	GND
12	GND	AD39	GND
13	AD37	AD36	GND
14	GND	AD32	GND
15	/REQ5*	/GNT5*	GND
16	GND	nc	GND
17	/REQ6*	/GNT6*	GND
18	GND	nc	GND
19	nc	nc	GND
20	GND	nc	GND
21	nc	nc	GND
22	GA1	GA0	GND

* driven only when assembled for and located in system slot

5.3 Front Panel Connector CON2

Table 8: shows the pin assignment of PCI Express External Cable Interface connector.

Table 8: Pin Assignment of the Front Panel Connector CON2

Pin No.	Signal	Signal	Pin No.
A1	CPER0_N	GND	B1
A2	CPER0_P	not connected	B2
A3	not connected	CWAKE#	B3
A4	SB_RTN	CPRSNT#	B4
A5	CFRECLK_N	GND	B5
A6	CFRECLK_P	not connected	B6
A7	not connected	CPWRON	B7
A8	CPERST#	CPET0_N	B8
A9	GND	CPET0_P	B9

5.4 DIL Switch SW1

The PI2EQX4402 implements four unidirectional ports, two of which are used on the **NcPCI-XLINK**. DIL switch SW1 is used to set the line transmission characteristics of ReDriver port B, which drives the PCIe line from the PCIe → PCI bridge to the PCI Express Cable Interface connector.

Table 9: Switch Assignment of DIL Switch SW1

Switch No.	Signal	Default Setting
Pos. 1	SEL_B0	on
Pos. 2	SEL_B1	on
Pos. 3	SEL_B2	on
Pos. 4	SEL_B3	on
Pos. 5	SEL_B4	on
Pos. 6	SEL_B5	off
Pos. 7	SEL_B6	off
Pos. 8	not used	on

5.5 DIL Switch SW2

The PI2EQX4402D implements four unidirectional ports, two of which are used on the **NcPCI-XLINK**. DIL switch SW2 is used to set the line transmission characteristics of ReDriver port C, which drives the PCIe line from the PCI Express Cable Interface connector to the PCIe → PCI bridge. It also includes a switch (pos. 8), which selects between PCI Express Cable Interface clock and a local clock oscillator as a reference for the PCIe → PCI bridge. By default, the PCI Express Cable Interface clock is selected.

Table 10: Switch Assignment of DIL Switch SW2

Switch No.	Signal	Default Setting
Pos. 1	SEL_C0	on
Pos. 2	SEL_C1	on
Pos. 3	SEL_C2	on
Pos. 4	SEL_C3	off
Pos. 5	SEL_C4	off
Pos. 6	SEL_C5	off
Pos. 7	SEL_C6	off
Pos. 8	PCIE_CLKSEL	off

The default settings for both switches SW1 and SW2 have been successfully tested with various cable lengths from 50cm to 7m and should work without change with most user applications.

6 Known Bugs / Restrictions

- ReDriver link sense circuitry not functional, link status not diplayed correctly on LEDs 1 and 2.

Appendix A: Reference Documentation

[1] Pericom, PI2EQX4402D 2.5Gbps x2 Lane Serial PCI Express Repeater / Equalizer with Signal Detect feature, 11/06
[2] PI7C9X111SL PCI Express-to-PCI Reversible Bridge, Rev. 1.0, October 2008
[3] PCI Local Bus Specification, Revision 3.0, February 3, 2004
[4] PCI-to-PCI Bridge Architecture Specification, Revision 1.2, June 9, 2003
[5] PCI-ISA Card Edge Connector for Single Board Computer, PICMG 1.0 R2.0, 2003
[6] PCI Express Base Specification, Revision 2.0, December 20, 2006
[7] PCI Express External Cabling Specification, Revision 1.0, January 4, 2007

Appendix B: Document's History

Revision	Date	Description	Author
1.0	02/17/2009	initial revision	ga